Reed Business Information (RBI™)

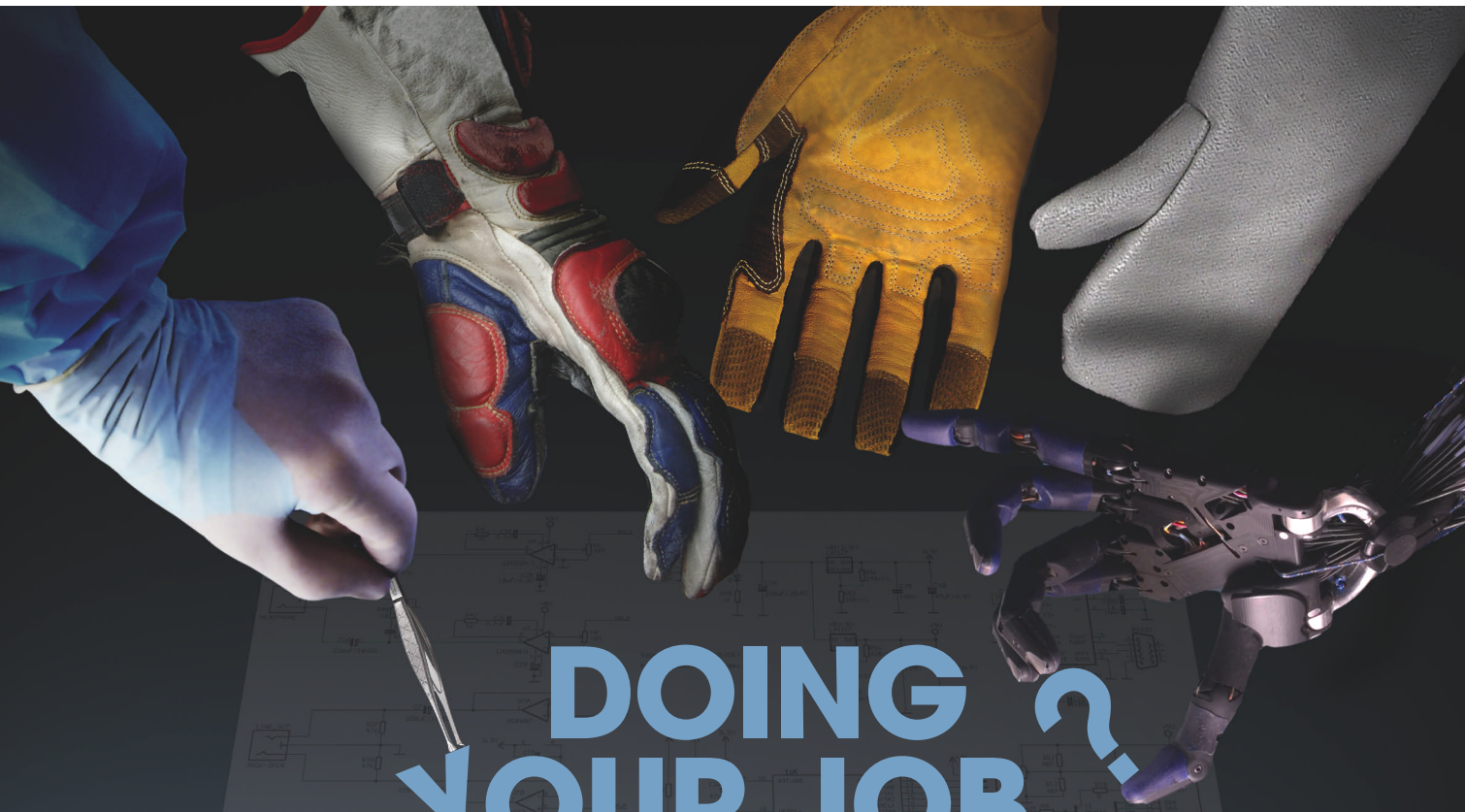
EDN

VOICE OF THE ENGINEER

JULY 9

Issue 13/2009

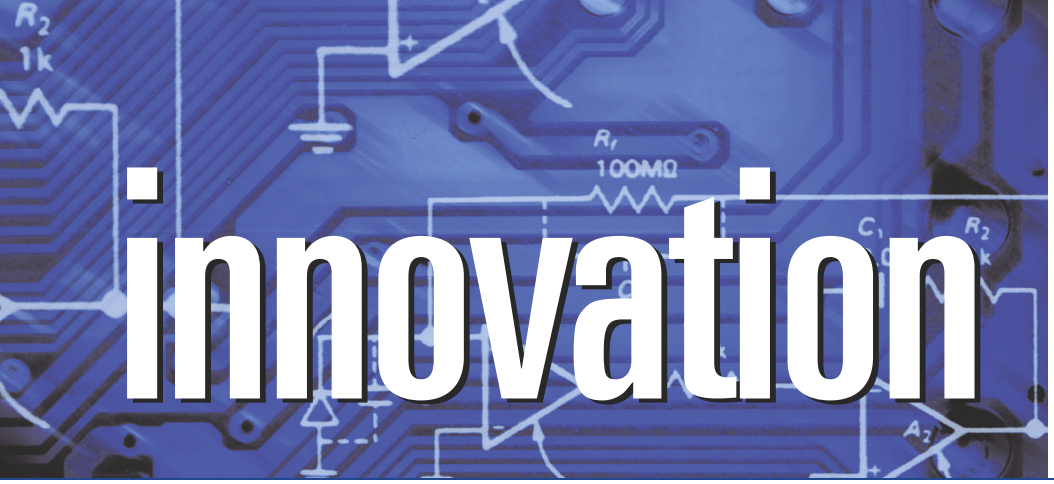
www.edn.com



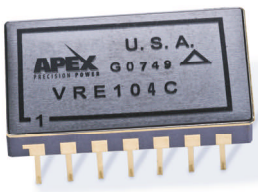
DOING YOUR JOB?

HIGH-LEVEL SOFTWARE FOR EMBEDDED-SYSTEM DESIGN

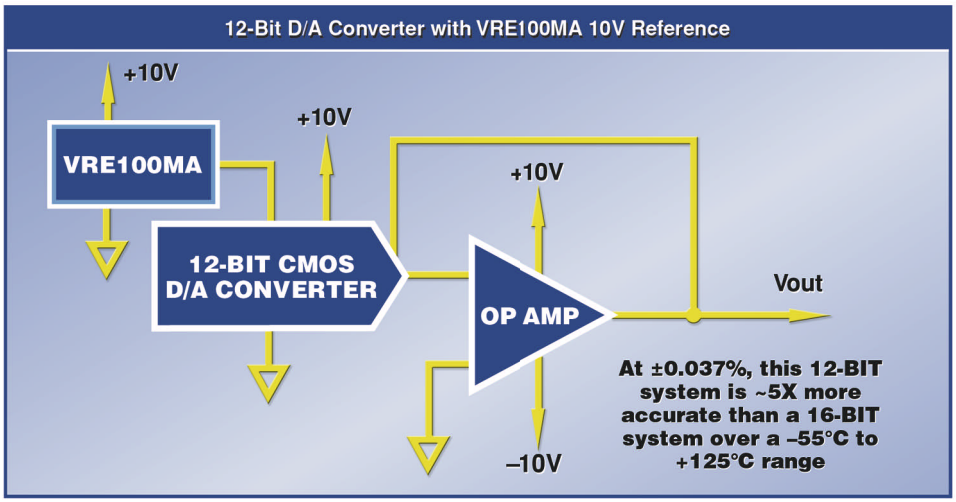
Page 20



APEX™
PRECISION POWER
Product Innovation from Cirrus Logic



VRE100 SERIES
DIP14 PACKAGE



Voltage References Deliver Precision Performance For Better Accuracy, Temperature and Thermal Management

Cirrus Logic's new family of precision voltage references offer performance features designed to minimize the impact of operating conditions.

This new VRE series of precision voltage references are designed to exhibit very low voltage drift and temperature coefficients, as well as reduced thermal hysteresis. "Precision" in nature, various package options provide additional pins for trimming or temperature monitoring. The result is an enhanced level of performance when compared with their nearest competition of functionally equivalent three-terminal voltage references.

Series	Output (V)	Initial Error (mV)	TempCo (ppm/°C)	Noise (µVpp)	Package	Feature
VRE100	+10, –10, ±10	0.5, 0.8, 1.0, 1.5	0.3, 0.5	6	DIP14	High Rel
VRE104	4.5	0.4, 0.8	0.4, 0.8	3	DIP14	Cirrus ADCs
VRE107	+5, –5	0.4, 0.8	0.4, 0.8	3	DIP14	High Rel
VRE117	+3	0.2, 0.3	0.3, 0.6	1.5	DIP14	Low Output V
VRE202	2.5	0.2, 0.3	0.4, 0.8	1.5	LCC20	Small Pkg
VRE204	4.5	0.4, 0.8	0.4, 0.8	3	LCC20	Small Pkg
VRE205	5	0.4, 0.8	0.4, 0.8	3	LCC20	Small Pkg
VRE210	10	0.3, 0.4, 0.5, 0.8	0.3, 0.5	6	LCC20	Small Pkg
VRE302	2.5	0.25, 0.4, 0.5	0.6, 1.0, 2.0	1.5	DIP8, SMT8	Low Cost
VRE304	4.5	0.4, 0.7, 0.9	0.6, 1.0, 2.0	3	SMT8	Low Cost
VRE305	5	0.5, 0.8, 1.0	0.6, 1.0, 2.0	3	DIP8, SMT8	Low Cost
VRE306	6	0.6, 1.0, 1.2	0.6, 1.0, 2.0	3	SMT8	Low Cost
VRE310	10	1.0, 1.6, 2.0	0.6, 1.0, 2.0	6	DIP8, SMT8	Low Cost
VRE405	±5.0	0.5, 0.8, 1.0	0.6, 1.0, 2.0	3	DIP14, SMT14	Dual, Low Cost
VRE410	±10.0	1.0, 1.6, 2.0	0.6, 1.0, 2.0	6	SMT14	Dual, Low Cost
VRE3025	2.5	0.2, 0.4, 0.5	0.6, 1.0, 2.0	1.5	DIP8, SMT8	+10V Supply
VRE3050	5	0.4, 0.7, 0.9	0.6, 1.0, 2.0	3	SMT8	+10V Supply
VRE4112	1.25	0.625	2.0, 3.0	2.2	SOIC8	Low Cost, 5V Supply
VRE4125	2.5	1.250	1.0, 3.0	2.2	SOIC8	Low Cost, 5V Supply
VRE4141	4.096	2.048	1.0, 3.0	2.2	SOIC8	Low Cost, 5V Supply

NORTH AMERICA
+1 800-625-4084

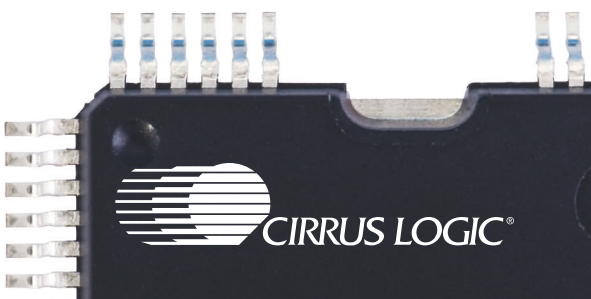
ASIA PACIFIC
+852 2376-0801

JAPAN
+81 (3) 5226-7757

EUROPE/UK
+44 (0) 1628-891-300

LEARN MORE AT
www.cirrus.com/vre

For product selection assistance or technical support with Apex Precision Power™ products call 1-800-546-2739 or tucson.support@cirrus.com.



Digi-Key® CORPORATION

SAME-DAY SHIPPING on orders entered by 8:00 pm central
NEXT-DAY DELIVERY

Over 400,000 products in stock from more than 400 supplier partners.*

The industry's broadest product selection available for immediate delivery

www.digikey.com

1.800.344.4539

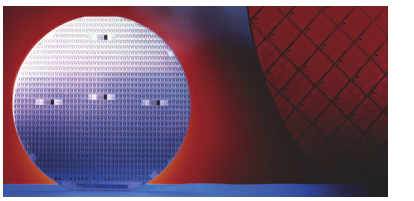
An additional 1,000,000+ components can be sourced at digikey.com

*Digi-Key is an authorized distributor for all supplier partners. New products added daily. © 2009 Digi-Key Corporation, 701 Brooks Ave. South, Thief River Falls, MN 56701, USA

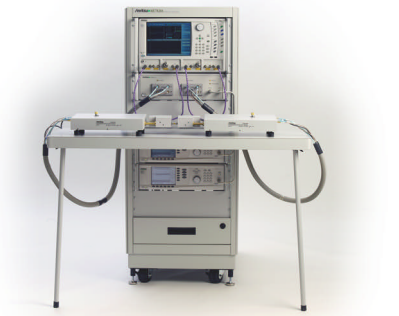
EDN 7.9.09 contents

High-level software for embedded-system design

FPGA verification in embedded video-processing systems



Small-delay-defect testing

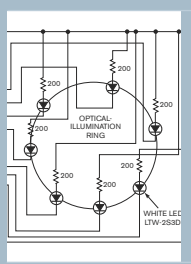


EDA companies tout RF design, links to test

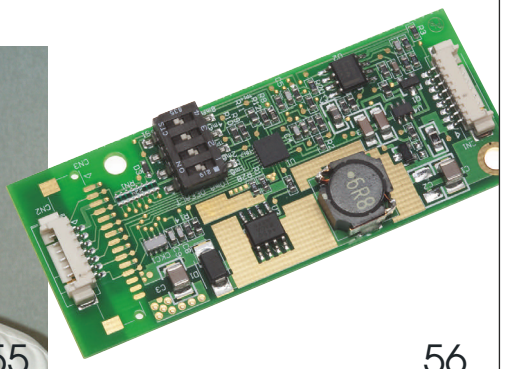
Early verification and validation using model-based design

pulse

DESIGNIDEAS



55



56

DEPARTMENTS & COLUMNS

EDN online contents www.edn.com

ONLINE ONLY

Check out these Web-exclusive articles:

Transformational change: the revolution to come in electronics design

Like the proverbial comet strike that wiped out the dinosaurs, the global recession has changed the climate for electronics. You'd better think about changing your organization's design culture—and maybe your corporate culture—to adapt.

➔www.edn.com/article/CA6665049

Characterize optocouplers in the feedback loop of high-frequency power converters

Optocouplers will add a phase shift that can make your power supply unstable. Here is how you can measure and compensate the loop.

➔www.edn.com/article/CA6666261

GUEST OPINIONS

In this area of EDN.com, vendors can discuss their strategies, views on design challenges, and product ideas directly with you, without the intervention of *EDN*'s editorial staff. These pieces represent the views of the author, not of *EDN* or its editors.

Here's a sample of recently posted guest opinions:

Closing the ESL gap

"In-design" physical verification is "on-time" physical verification

One size fits all

Innovating out of the downturn

➔www.edn.com/guestopinions

EDN® (ISSN#0012-7515), (GST#123397457) is published biweekly, 24 times per year, by Reed Business Information, 8878 Barrons Blvd, Highlands Ranch, CO 80129-2345. Reed Business Information, a division of Reed Elsevier Inc, is located at 360 Park Avenue South, New York, NY 10010. Tad Smith, Chief Executive Officer; Mark Finkelstein, President, Boston Division. Periodicals postage paid at Littleton, CO 80126 and additional mailing offices. Circulation records are maintained at Reed Business Information, 8878 S Barrons Blvd, Highlands Ranch, CO 80129-2345. Telephone (303) 470-4445. POSTMASTER: Send address changes to EDN®, PO Box 7500, Highlands Ranch, CO 80163-7500. EDN® copyright 2009 by Reed Elsevier Inc. Rates for nonqualified subscriptions, including all issues: US, $179.99 one year; Canada, $229.99 one year (includes 7% GST, GST#123397457); Mexico, $229.99 one year; air expedited, $399.99 one year. Except for special issues where price changes are indicated, single copies are available for $10 US and $15 foreign. Publications Agreement No. 40685520. Return undeliverable Canadian addresses to: RCS International, Box 697 STN A, Windsor Ontario N9A 6N4. E-mail: Subsmail@ReedBusiness.com. Please address all subscription mail to EDN®, 8878 S Barrons Blvd, Highlands Ranch, CO 80129-2345. EDN® is a registered trademark of Reed Elsevier Properties Inc, used under license. A Reed Business Information Publication/Volume 54, Number 13 (Printed in USA).

EDN

EDN, 225 Wyman St, Waltham, MA 02451. **www.edn.com**. Phone 1-781-734-8000. **Address changes or subscription inquiries:** phone 1-800-446-6551; fax 1-303-470-4280; subsmail@reedbusiness.com. For a free subscription, go to **www.getfreemag.com/edn**. Reed Business Information, 8878 S Barrons Blvd, Highlands Ranch, CO 80129-2345. Include your mailing label.

Reed Electronics Group

BY RICK NELSON, EDITOR-IN-CHIEF

Design mingles with test across domains

The lines between electrical-engineering disciplines are continually blurring, with traditional test products taking on design chores and vice versa. The lines between electronics engineers and experts in other domains may be blurring, as well. This issue's cover story highlights both of these trends; it recounts the efforts of design and test companies and their customers to bring medical and aerospace systems to market. Increasingly, domain experts in fields such as medical electronics, aerospace engineering, and mechatronics can participate in tasks once the province of C coders or hardware engineers.

A similar blurring of lines within the electrical-engineering field itself was evident at the IEEE MTT-S (Institute of Electrical and Electronics Engineers Microwave Theory and Techniques Society) IMS (International Microwave Symposium), which took place last month in Boston. There, EDA companies including AWR highlighted links to instrument makers such as Rohde & Schwarz (see "EDA companies tout RF design, links to test," *EDN*, this issue, pg 35). National Instruments, which has been promoting its LabView product as a design tool, demonstrated a LabView-generated program controlling WiMax test on a PXI (peripheral-component-interconnect-extensions-for-instrumentation) system.

Nevertheless, focus remains important. Although Agilent Technologies demonstrated both design and test products at the IMS, Darlene JS Solomon, chief technology officer and vice president of Agilent Labs, indicated the company's true center of attention in a presentation during the show titled "A singular focus on measurement." Solomon noted that Agilent has been serving the RF/microwave industry for more than 60 years, having introduced a signal generator in 1943. Agilent's offerings have expanded drastically over the years, she said. The company has tested more than half of the world's cell phones and addresses such far-flung application areas as food and water safety, medicine, crime prevention, and disease research.

"To measure is to know," she said, attributing the quotation to Scottish physicist James Clerk Maxwell, although others have attributed it to British mathematician and physicist Lord William Kelvin. Solomon also referred to US computer scientist Admiral Grace Murray Hopper, who said, "One accurate measurement is worth a thousand expert opinions." Solomon didn't draw a direct link between design and test, but she did link science and measurement, saying "Science is inextricably linked to new measurement tools," with measurement advances driving advances in fundamental knowledge. These advances in turn drive technology improvements and enable additional measurement advances in a virtuous circle.

Solomon also discussed new measurement modalities in which electrical, physical, chemical, and biological measurements, once the domain of their respective and exclusive sets of instrumentation, are converging, especially at the nanoscale. "Biology is all about complexity and has been functioning at the nanoscale for billions of years," she said. "Now, we can begin to measure and understand that complexity." That complexity has implications for both biology and electronics.

"Convergence implies multimodal measurement," Solomon added, explaining that Agilent's new scanning microwave microscope permits surface-topography measurements and supports the investigation of electrical properties at the surface and even below the surface, thereby enabling evaluation of semiconductor materials without destructive analysis.

"Measurement is integral to our technology-surrounded lives," she said. That proposition is one that we all can agree on, whatever our domains of expertise. EDN

"Measurement is integral to our technology-surrounded lives."—Darlene JS Solomon

Contact me at rnelson@reedbusiness.com.

MEET THE GUY that ELIMINATED HIS TEAM'S MANUFACTURING VARIABILITY ISSUES.

FIX YOUR MANUFACTURING VARIABILITY PROBLEMS AND YOUR REPUTATION WILL PRECEDE YOU. If you're designing chips for high functionality, high speed and lower power consumption at the most advanced process nodes, you've got variability issues. We have the solution that will increase your yield, performance and prestige by a wide margin. | Get more information at mentor.com/solutions/manufacturing-variability.

Mentor Graphics®

THE EDA TECHNOLOGY LEADER

EDITED BY FRAN GRANVILLE

pulse

INNOVATIONS & INNOVATORS

Arbitrary-waveform generator combines protocol- and physical-layer testing

The need is intensifying to investigate and identify performance impairments resulting from imperfections in the physical layers of serial buses such as Flexray, an advanced data-transmission technology for communication among the many intelligent subsystems in modern motor vehicles. As cars and trucks that incorporate such subsystems reach the roads in growing numbers, the lives of more and more people will depend on the reliable performance of these systems. Now, Agilent Technologies has found a way to merge physical-layer and protocol testing of such buses and has incorporated the capability in a $3990 pattern-generator option, which the company is offering for its 81150A 1-µHz to 120-MHz pulse/function/pseudorandom-noise/arbitrary-waveform generator, whose US base prices begin at $9000.

Already a Swiss Army Knife of waveform generators, the 120-MHz 81150A can now also perform protocol/physical-layer testing of advanced serial buses if you upgrade its internal software to activate a pattern-generator option.

With the option, the instrument allows pass-through of patterns for combined physical-layer and protocol testing at rates as high as 10 Mbps and can produce arbitrary bit-shaped patterns that emulate overshoot, asymmetric delay, and duty-cycle distortion at rates to 120 Mbps. Agilent implemented the option in software, and activating the upgrade also unlocks built-in 16-bit-wide pattern memory. Owners of some older units must download and install a free software revision before they can activate the upgrade.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com/find/81150.

FEEDBACK LOOP

"You blamed the intern?!!! I hope you're just kidding. There is no way the poor schmuck could be expected to know the difference between CA3127 and HFA3127 unless you specifically warned against it at the outset. ... Oh, if you were just kidding, then never mind."

—*EDN* reader and RF engineer Kirt Blattenberger, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6607211. Add your comments.

Ramtron expands serial-FRAM line with 32-kbit device

Ramtron International Corp, a supplier of nonvolatile FRAM (ferroelectric random-access memory), has announced the FM24CL32, a serial-nonvolatile RAM that offers high-speed read/write performance, low-voltage operation, and long-term data retention. The FM24CL32 features 32-kbit nonvolatile memory organized in a 4096-word×8-bit array. It comes in an 8-pin SOIC package that uses the two-wire I^2C (inter-integrated-circuit) protocol. The FM24CL32 features fast read/write access. Unlike an EEPROM, it exhibits no write delays and requires no data polling. The device writes at bus speeds as high as 1 MHz and supports legacy speeds of 100 and 400 kHz.

The FM24CL32 withstands 10^{14} read/write cycles. It operates from a 2.7 to 3.6V supply and typically draws 70 µA at 100 kHz when active and 12 µA in standby. The device is a direct hardware replacement for serial EEPROM in industrial-control, metering, medical, military, gaming, and computing applications. It provides reliable data retention for 45 years when you operate it at 75°C, a necessary retention time for the utility-metering industry. The FM24CL32 operates over the industrial-temperature range of −40 to +85°C. Unit prices begin at 99 cents (10,000).

—by Rick Nelson

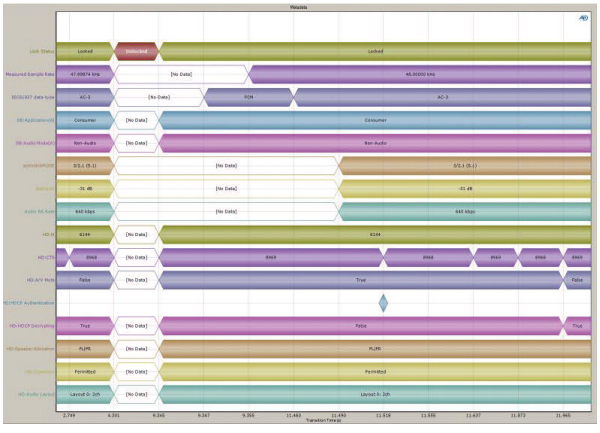
▷**Ramtron International Corp**, www.ramtron.com.

Software upgrade brings logic-analyzer-style insights to audio testing

Audio Precision has announced several new features for its APx series of audio analyzers. These features relate to the display, analysis, and control of metadata in HDMI (high-definition-multimedia interface); IEC (International Electrotechnical Commission) 60598 standard, which defines the Toslink and S/PDIF (Sony/Philips digital-interface format) consumer digital-audio interfaces; and AES3/EBU (Audio Engineering Society 3/European Broadcast Union) digital-audio streams. The additional features are available in the first beta release of APx500 Version 2.4 software. The vendor expects to release the full Version 2.4 this year. "Errors in metadata can cause real problems in HDMI that you just don't see in S/PDIF," explains Dan Knighten, Audio Precision's director of products. "A logic-analyzer view shows exactly what's going on over time so you can identify what's causing glitches or other issues."

Three features of the new release, including two new metadata monitors, relate to the analysis and management of metadata. One of these monitors allows decoding and displaying the entire HDMI audio InfoFrame, including the current values of CTS (cycle-time stamp) and N, a constant that CTS uses to define the relationship between the audio-sample clock and an HDMI link's TMDS (transmission-minimized-differential-signaling)-master-clock values, HDCP (high-bandwidth-digital-content-protection) state, audio layout, and audio/video-mute condition. The second monitor displays information about the channel status and user bits embedded in IEC60958/AES3/EBU-format audio content. Both the HDMI and the IEC60598 audio monitors also display the digital-audio stream type and sample rate, as well as Dolby and DTS (Digital Theatre Sound) parameters, including the dialogue-normalization level, bit rate, and ACmod/Amode values. ACmod for Dolby and Amode for DTS are metadata that define a bit stream's number of encoded channels.

Two new metadata-editor panels allow you to override default metadata settings and set channel-status information and HDMI audio-InfoFrame data to any value. You can use these panels to verify the response of a device under test to both valid and invalid settings. The metadata recorder is an easy-to-read color display, which, in a logic-analyzer-like display, can plot the changing states of multiple metadata fields in real time. You can simultaneously display as many as 15 fields, so you can monitor in detail what happens to metadata when you hot-plug an HDMI device, or you can determine when and where data glitches occur in a corrupted audio stream. The system also automatically identifies and flags discrepancies between the indicated metadata and the received metadata—for example, if the input sample rate is 48 kHz but the channel status indicates that it should be 44.1 kHz. The results of such measurements are helpful in verifying that a device under test's behavior complies with relevant specifications.



According to Audio Precision, no better method exists for troubleshooting problems with digital-audio metadata than this logic-analyzer-like presentation, available in new software for the APx series of audio analyzers.

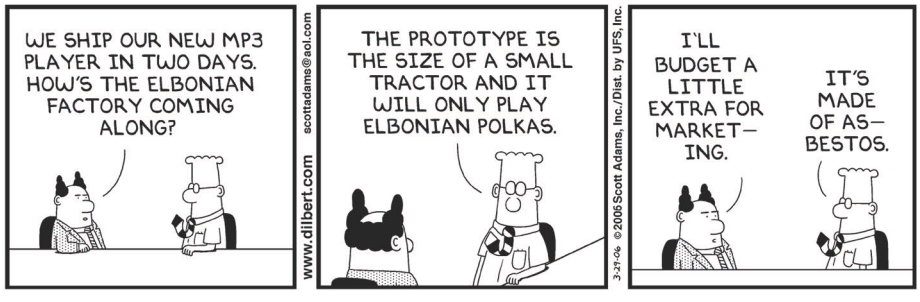
> Two new metadata-editor panels allow you to override default metadata settings and set channel-status information.

APx's US prices start at less than $10,000 for the hardware and required software. You can download the free APx 2.4 beta release with the above-noted features at http://ap.com/beta. Taking advantage of Version 2.4's digital-protocol-analysis features requires digital-I/O hardware, which the APx525 includes at its US price of $12,250.

—by Dan Strassberg

▷**Audio Precision**, http://ap.com/products/apx.

DILBERT By Scott Adams



SIwave 4.0 addresses signal and power integrity

Part of the Ansys Ansoft (www.ansoft.com) family of products, SIwave (signal-integrity-wave) Version 4.0 includes new features for signal-integrity, power-integrity, and electromagnetic-compatibility testing. Enhancements include an improved desktop graphical user interface, access to post-processing results, and solver enhancements that provide accurate results beyond 10 Gbps. In addition, you can now automatically link SIwave electromagnetics with circuit simulation using the Ansoft Nexxim circuit-simulation and -analysis software and Ansoft Designer schematic- and design-management front end. To account for board and package thermal effects, a new link through Ansys Icepak software enables accurate characterization of additional heating due to copper-resistive losses that engineers have previously estimated or ignored.

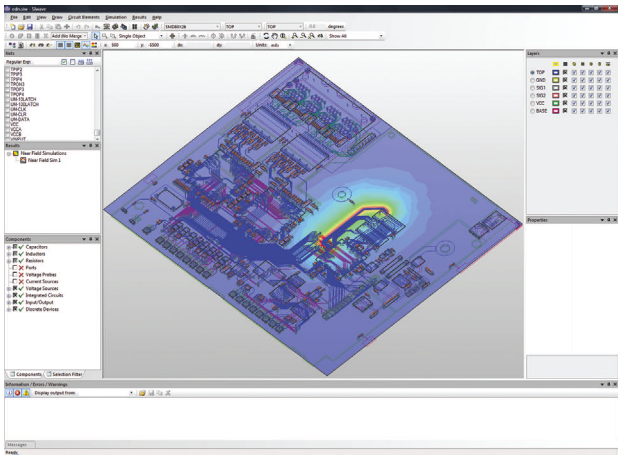
> The release includes multiple automation enhancements that ease design flows.

The SIwave electromagnetic-field solver performs broadband signal- and power-integrity and dc-voltage and current analysis for boards and packages. SIwave software offers electromagnetic-interference and compatibility analyses, and it can couple board and package electromagnetic fields with HFSS (high-frequency-simulator-system), 3-D, full-wave electromagnetic-field-simulation software for system-level simulation (see "Simulation gets speed, capacity boost," *EDN*, Jan 22, 2009, pg 26, www.edn.com/article/CA6629472).

SIwave features an enhanced graphical user interface that eases component management and allows simultaneous analyses and dynamic zooming. A new reporter feature eases and speeds the analysis of results. Improved solver enhancements include smart coupling algorithms with an advanced via solver and nonuniform hexagonal- and trapezoidal-trace cross-sections that provide accurate results at speeds greater than 10 Gbps. A new coplanar algorithm within the solver extends accuracy for difficult package designs, and a new field solver provides on-the-fly calculations of trace characteristics. Enhanced near- and far-field solvers address electromagnetic-interference and compatibility problems for data-dependent fields when you link them to circuit simulation using Ansoft Designer software.

The release includes multiple automation enhancements that ease design flows by removing tedious manipulations that you would otherwise have to perform manually. SIwave incorporates automated error checking and geometry correction. Using the new version with Ansoft Designer provides automated schematic creation and electromagnetic-driven transient- and QuickEye-analysis setups for circuit simulation. The technology now also allows native merging of packages to PCBs (printed-circuit boards). SIwave also uses the provided header information to automatically create ports for Apache (www.apache-da.com) RedHawk chip power modules.**—by Rick Nelson**

▷**Ansys**, www.ansys.com.



Ansys' SIwave Version 4.0 includes features for signal-integrity, power-integrity, and electromagnetic-compatibility testing. The image shows a plot of the magnetic-field magnitude above a PCB when a sinusoidal source drives a line at 1 GHz.

DEVELOPER'S GUIDE DETAILS USB 3.0, SUPERSPEED

USB Complete: The Developer's Guide **by Jan Axelson, author of many books on embedded-system development, is now in its fourth edition. With little question, hardware and software developers have recognized the earlier editions as the most authoritative, readable, and indispensable compilations of information on what has to be the 21st century's most ubiquitous peripheral bus. But with the advent of USB (Universal Serial Bus) 3.0 and its Superspeed capability, Axelson decided to write a new edition (Lakeview Research, June 2009, ISBN: 978-1931448086).**

You might wonder whether a 504-page book on USB whose index lists only 20 pages of material on USB 3.0 and Superspeed provides adequate coverage of the bus' latest capabilities. For many readers, it almost certainly does so, although the author provides frequent updates at www.lvr.com.

If you are not yet developing USB 3.0/Superspeed products, the USB 3.0 frequently asked questions of the Web site, which you can also find on pg 27 of the $54.95 book, may provide all of the answers you are looking for.

—by Dan Strassberg

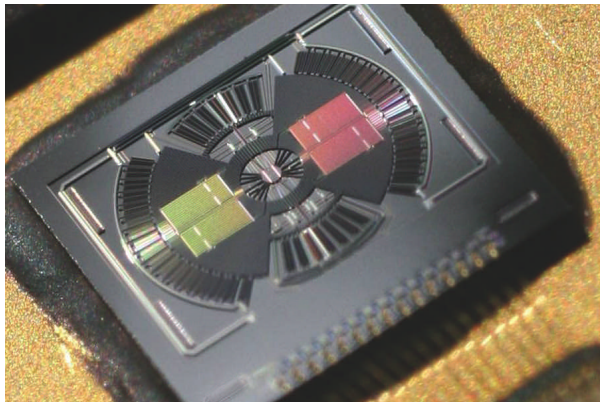
▶**Lakeview Research, www.lvr.com.**

MEMS-based motion sensors move lower in both size and price

The 16-bit, three-axis LIS-302DLH digital MEMS (microelectromechanical-system) accelerometer from STMicroelectronics is 0.75 mm high and has a 3×5-mm footprint. It has a power-saving shutdown mode and wakes automatically when it detects motion.

The integrated digital circuitry provides acceleration measurements to ±8g through an I^2C (inter-integrated-circuit)/SPI (serial-peripheral-interface)-bus interface, allowing direct connection to the system processor with no external components required. The device sells for $1.35 (10,000).

STMicro has also introduced a family of single-axis and multiaxis MEMS gyroscopes that offer a full-scale range of 30 to 6000°/sec. The sensors simultaneously provide two separate outputs for each axis, including an unamplified output for general detection of angular motion and 4× amplification for high-resolution measurements.



The new LIS302DLH family of single-axis and multiaxis MEMS gyroscopes offers a full-scale range of 30 to 6000°/sec and can operate with a supply voltage of 2.7 to 3.6V.

The gyroscopes are stable over a wide temperature range and time, with variation typically lower than 0.05°/sec/°C for zero-rate level, eliminating the need for further temperature compensation in the application. The noise level at the output signal—0.014°/sec/$\sqrt{Hz}$ at 30°/sec full-scale—does not affect measurement precision. The devices can operate with any supply voltage of 2.7 to 3.6V and come in a 5×5-mm LGA package.

Two members of the new family are the LPR503AL, a two-axis pitch-and-roll gyroscope with 30 and 120°/sec full-range scales, and the LPY550AL, a two-axis pitch-and-yaw gyroscope with 500 and 2000°/sec full-scale ranges. The devices sell for $2.50 (10,000 or more).

—by Margery Conner

▷**STMicroelectronics**, www.st.com/mems.

TOOL TARGETS INCREASED PRODUCTIVITY IN ANALOG ENVIRONMENT

Synopsys recently announced the addition of advanced analog-simulation and -layout capabilities in its Galaxy Custom Designer implementation tool. The new features in the 2009.06 release target analog-circuit designers and -layout engineers. The new capabilities include high-capacity, high-performance SDL (schematic-driven layout) for today's large analog blocks. The SDL capability features robust schematic- and layout-synchronization technology and a streamlined ECO (engineering-change-order) flow. The 2009.06 release also includes an easy-to-use analog-simulation and -analysis environment featuring high-performance waveform display and processing, mixed text/schematic integration, and TCL (Tool Command Language) scripting for batch verification.

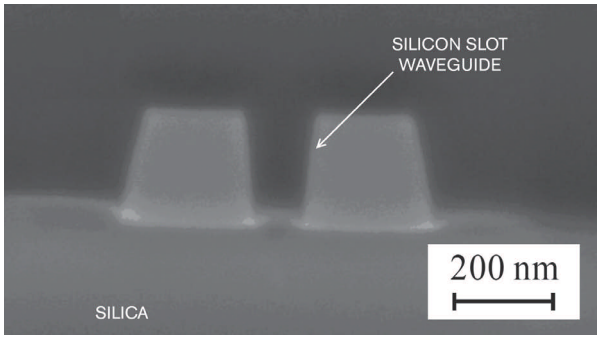
Previewing the release at IMS (International Microwave Symposium, www.ims2009.org) last month, Ed Lechner, director of product marketing for custom design at Synopsys, said that the new release builds on the Custom Designer version that Synopsys released in September 2008. The overall goal is to increase productivity for custom designs in an open environment as process geometries shrink to 45 nm and below. According to Lechner, Custom Designer offers time-saving analysis setup, run, save, and recall features; it provides hierarchical mixed-text and schematic representations; and it supports cross-probe and schematic annotation with simulation results. It forms the basis of a complete implementation, physical-verification, circuit-simulation, and analysis flow, integrating with HSpice, Custom Explorer, Cadabra, IC Validator, StarRCXT, and CustomSim.

Synopsys' RF-design capabilities include design, analysis, modeling, and extraction tools as well as RF IP (radio-frequency intellectual property). Lechner describes an RF flow using Custom Designer for schematic capture, HSpice RF for circuit simulation, Custom WaveView for analysis, Custom Designer for layout, IC Validator for design-rule checking, StarRCXT for parasitic extraction, and CustomSim for verification. Other relevant tools include TCAD (technology computer-aided design) for device modeling. HSpice RF supports harmonic balance and shooting-Newton techniques for analysis of weakly and strongly nonlinear devices, respectively. It also supports envelope analysis for complex modulated RF waveforms and S-parameter analysis for small-signal, linear components. It can simulate more than 10,000 active devices, and you can use it for signal-integrity simulations of transmission lines.

—by Rick Nelson

▶Synopsys, www.synopsys.com.

07.09.09



This cross-section shows the vapor-deposited organic film covering the silicon waveguide. The waveguide is patterned on a silicon-on-insulator substrate (courtesy IMEC).

RESEARCH UPDATE

EDITED BY RON WILSON

Advance hints at all-optical add-drop multiplexers

A recent breakthrough at the University of Karlsruhe (www.uni-karlsruhe.de), in collaboration with IMEC (Interuniversity Microelectronics Center), Lehigh University (www.lehigh.edu), and ETH (Swiss Federal Institute of Technology) Zurich (www.ethz.ch), has demonstrated optical demultiplexing at speeds greater than 100 Gbps. Until this breakthrough, as bit rates in the optical backbone sped past 40 Gbps per wavelength, a fundamental problem arose with the front-end optical-to-electronic conversion.

Converting an optical-pulse train at speeds higher than 40 Gbps to electronic pulses is a daunting prospect, according to Roel Baets, head of the photonics research group at IMEC. A better approach would be to optically demultiplex the bit stream, producing and then converting several lower-rate bit streams. Such a demultiplexer would require an optical-switching device that could operate synchronously at speeds greater than 100 Gbps.

Achieving this speed would require a material that is nonlinear with respect to light energy—that is, a material that changes its refractive index based on its light-energy density. In such a material, one light pulse could change the propagation method for a second pulse.

The researchers reasoned that, if they created a silicon slotted waveguide with a slot width of only approximately 100 nm and then deposited such a nonlinear organic material inside the waveguide, they would have created a very fast optical switch.

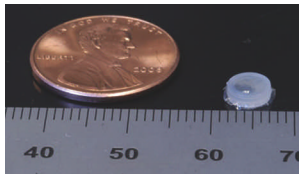
According to Baets, researchers directed an optical data-pulse stream—at 170 Gbps, in this case—into the waveguide. Then the researchers superimposed a stream of clock pulses of the same pulse width but at one-quarter the frequency and in-phase with the data-pulse stream. When a data pulse coincides with a clock pulse, the increase in optical energy alters the refractive index of the optical material.

In slotted waveguides, if the optical wave is polarized so that the electric field is horizontal, the field will be stronger in the lower-index material. When pulses coincide and change the refractive index of the organic material, this change of refractive index in effect moves the light back and forth between the organic material inside the waveguide and the silicon ridges that define the edges of the waveguide. In this way, much like a time-domain demultiplexer, the waveguide passively extracts the data pulses that coincide with the clock pulses—every fourth pulse—from the rest of the data-pulse train.**—RW**

▷**IMEC**, www.imec.be.

Implantable sensor device promises continuous cancer monitoring

Researchers at the Massachusetts Institute of Technology claim that they can implant a sensor device during a cancer-tissue biopsy and that the sensor can remain in patients for continuous monitoring of the disease's impact on their health. The device repeatedly samples the local environment for tumor-biomarker, chemotherapeutic-agent, and tumor-metabolite concentrations, which could improve early detection of metastasis and personalized therapy. "This [technique] basically takes the lab and puts it into the patient," says Michael Cima, MIT professor of materials science and engineering and an investigator at the David H Koch Institute for Integrative Cancer Research at MIT.



This cylindrical, 5-mm implant contains magnetic nanoparticles.

The cylindrical, 5-mm implant contains magnetic nanoparticles coated with antibodies specific to the target molecules. Target molecules enter the implant through a semipermeable membrane, bind to the particles, and cause them to clump together—a process that MRI (magnetic-resonance-imaging) procedures can detect. The device is made of polyethylene, a polymer that commonly finds use in orthopedic implants. The semipermeable polycarbonate membrane allows target molecules to enter but keeps the magnetic nanoparticles from exiting.

Researchers transplanted human tumors into mice and then used the implants to track levels of human chorionic gonadotropin, a hormone produced by human-tumor cells, over the course of a month. MRI detected that the transverse-relaxation time of devices in tumor-bearing mice after one day was 20±10% lower than devices in control mice. Researchers describe their findings in a recent study (**Reference 1**). For more, go to www.edn.com/article/CA6658480.

—by Suzanne Deffree

▷**Massachusetts Institute of Technology**, www.mit.edu.

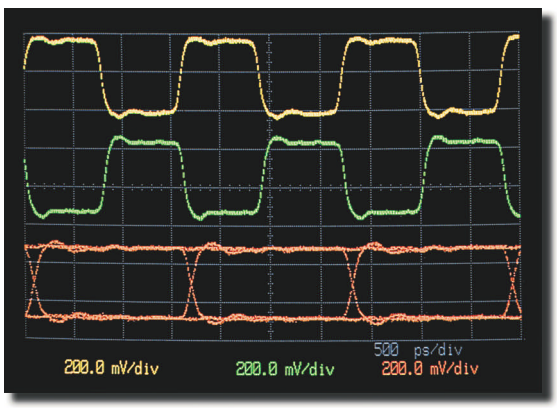
REFERENCE

1 Daniel, Karen D, et al, "Implantable diagnostic device for cancer monitoring," *Biosensors & Bioelectronics*, www.sciencedirect.com.

2 GHz Clock Generator

CG635...$2490 *(U.S. list)*

- ***Square wave clocks from DC to 2.05 GHz***
- ***Random jitter <1 ps (rms)***
- ***80 ps rise and fall times***
- ***16-digit frequency resolution***
- ***CMOS, LVDS, ECL, PECL, RS-485***
- ***Phase adjustment & time modulation***



Plot shows complementary clocks and PRBS (opt. 01) outputs at 622.08 Mb/s with LVDS levels. Traces have transition times of 80 ps and jitter less than 1 ps (rms).

The CG635 generates clock signals—flawlessly. The clock signals are fast, clean and accurate, and can be set to standard logic levels.

How fast? Frequency to 2.05 GHz with rise and fall times as short as 80 ps.

How clean? Jitter is less than 1 ps and phase noise is better than –90 dBc/Hz (100 Hz offset) at 622.08 MHz.

How accurate? Using the optional rubidium timebase, aging is better than 0.0005 ppm/year, and temperature stability is better than 0.0001 ppm.

You would expect an instrument this good to be expensive, but it isn't. You no longer have to buy an rf synthesizer to generate clock signals. The CG635 does the job better—at a fraction of the cost.

Stanford Research Systems

Phone: (408) 744-9040 · Fax: (408) 744-9049 · info@thinkSRS.com · **www.thinkSRS.com**

BY HOWARD JOHNSON, PhD

Holding on

Switch the CMOS-driver model high in **Figure 1** by closing S_1 and opening S_2. Wait for the line to settle. Because there is no dc load—only capacitance—the steady-state current equals almost zero. It differs from zero only according to the tiny leakage currents associated with the driver, the receiver, and the transmission line itself.

After settling, if you tristate the driver by opening S_1, the line remains in its high state, drifting slowly according to the leakage.

In practical terms, you can sometimes obtain many nanoseconds of dependable storage time in the tristate mode. The tristate feature, if available in your driver, acts as a sort of additional short-term dynamic-memory element that you can use to extend the hold time of your driver. It is just as reliable as any other DRAM circuit because it uses the same principle. The main difficulty is obtaining reliable information about the worst-case leakages. If you want to test the leakage, remember that leakage in the driver circuit grows exponentially with temperature, so test the circuit when it's hot.

The following example illustrates a situation in which a tristate technique might be helpful. Imagine two synchronous master-slave latches that the same 10-MHz synchronous clock drives. One, D_{OUT}, feeds data to the other. They both operate on the positive clock edge. At that speed, assuming modern CMOS logic, the circuit probably enjoys plenty of setup-timing margin but may lack hold margin, especially if the first device is much faster than the second.

The receiving latch may require more hold time than the transmitting latch guarantees. To expand the hold time on D_{OUT}, you may delay the clock feeding the transmitting device, insert a delay in series with the transmitted datapath, or invoke the tristate condition on the transmitter for a brief interval before and after each clock edge to prevent the output from changing until the required hold time for the receiving latch expires. Note that the output goes tristate when the control signal is high.

Before disabling the output, you must wait for the line to settle completely. Should the device enter the tristate condition while the line harbors any significant reflections, those reflections will bounce off C_{OUT} at the driver and C_{IN} at the load, and they thereafter ring back and forth in a highly resonant fashion. The residual ringing may persist into the critical timing zone. The source termination cannot prevent that type of ringing, not even if it is a perfectly laser-trimmed polysilicon resistor, because, during the tristate condition, the resistor no longer leads through a closed switch to a low-impedance power rail. It just leads to C_{OUT}. The source resistor works as a termination only when the driver is enabled. As a result, you must first wait for the line to settle and then invoke the tristate mode.

In some circumstances, tristating a line can exacerbate your difficulty with crosstalk or susceptibility to ESD (electrostatic discharge). Check for those conditions when the driver is active and when it is in the tristate condition. EDN

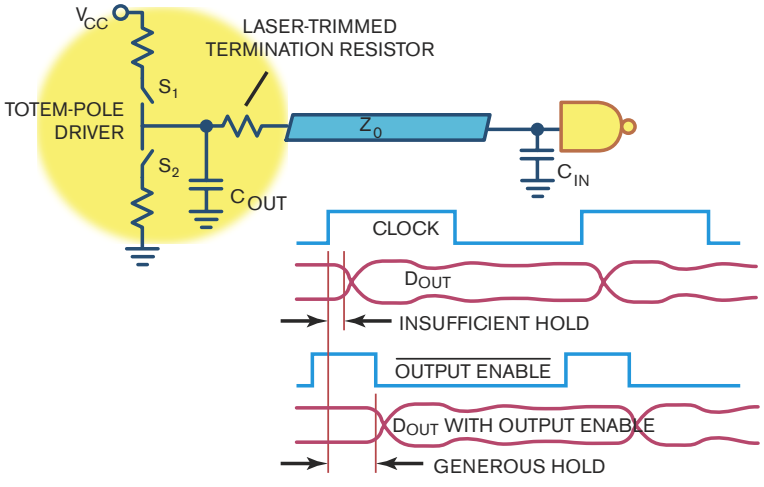
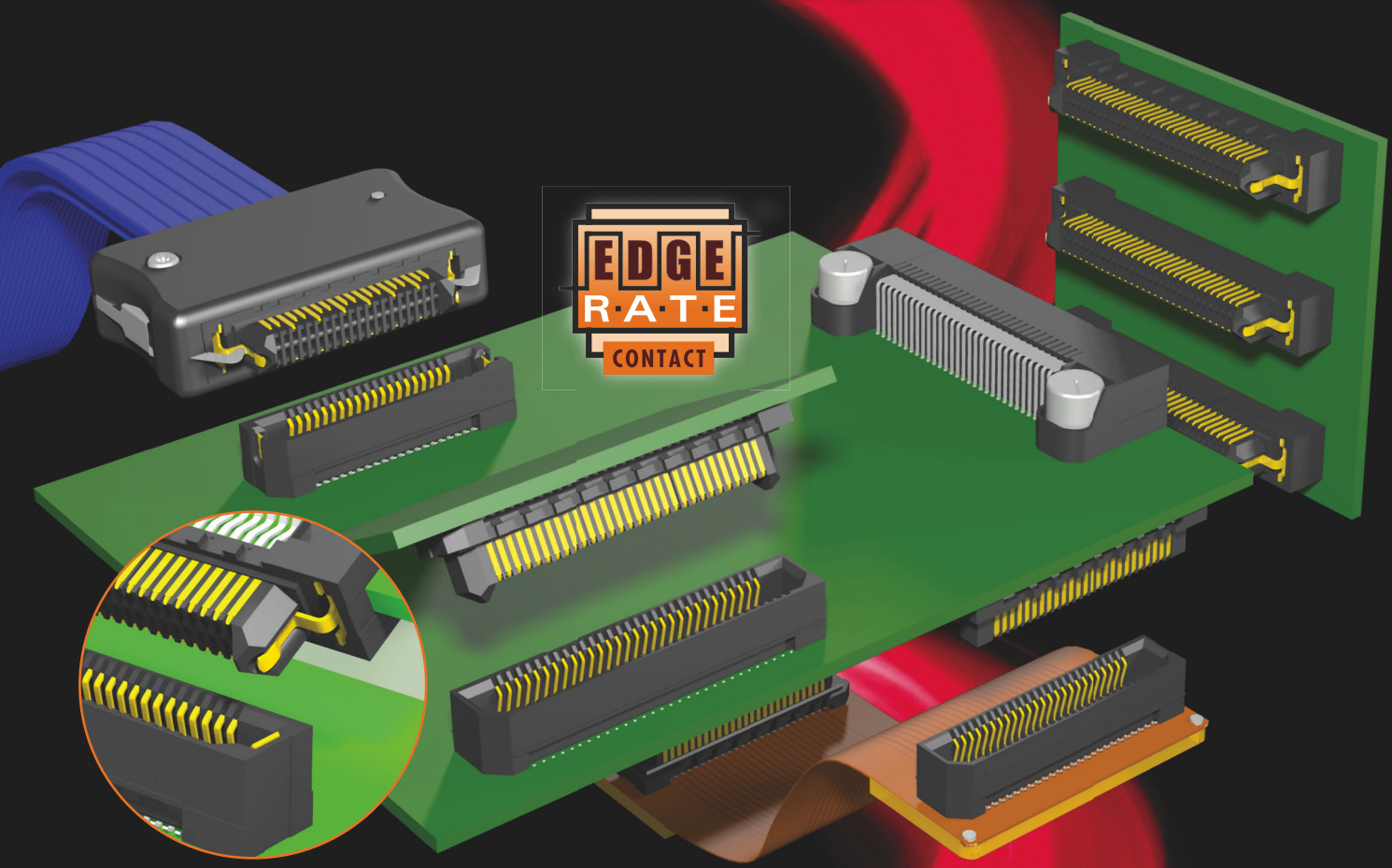


Figure 1 Clever timing can extend the D_{OUT} hold time.

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com.

The path of least resistance



...for rugged signal integrity.

- *Edge Rate*™ contact system on .8mm pitch is robust when zippered during unmating
- Rated at 9.5 GHz in differential pairs
- High speed cable assemblies, flex data links and RF cable solutions
- Right-angle and edge mount designs ideal for Micro Backplane applications

samtec

TRANSMISSION LINE SOLUTIONS

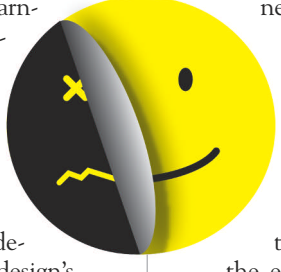
www.samtec.com/tls

BY PALLAB CHATTERJEE, CONTRIBUTING TECHNICAL EDITOR

Automation and the smiley face of death

The pervasive trends of manpower reduction and the shift toward the use of foundry services have created a new set of challenges for designers attempting to bring a prototype design to reality. The manufacturing-transfer process has gone from one with engineering oversight to one of almost complete automation. Although this automation allows for consistency in data structure and format and represents an attempt at minimal conformance to a set of design rules, it does not necessarily account for engineers' waivers and designers' assumptions and interpretation of the rules.

One demonstration of this trend is a design submission that "passes" an automated test and receives a "smiley face" indicating that the design transferred with no errors. More than 90% of the time, when a design has zero errors, there are a significant number of warnings. These warnings are lists of processing assumptions the automated-transfer process used to verify conformance to the design rules and tapeout guidelines. These warnings also include the design's data objects; the design's data layers; and information that the processing routines are ignoring, discarding, or both.



In most cases, if a design earns a smiley face, people release it to production without reading and understanding the impact or the extent of the warnings. But most designs with zero errors and multiple warnings end up functioning improperly and require many re-spins to fix. This issue is responsible for about 70% of design respins and presents the greatest challenge to product engineering on failure analysis. The product-engineering and yield-improvement groups are working from the assumption that the released design was correct relative to the design data, but the discrepancy between the actual released design and the engineering design can be significant.

Design transfer is no longer an engineering task but a collaborative effort.

In addition, most of the designs have a known block that does not conform to the designs' rules for devices. This block, usually called the "graffiti cell," contains the chip name, the copyright information, and other data. These contents are not operating devices. They identify the chip and the data sets that make it through testing. The foundry's incoming-data procedure should be able to identify and exclude checking of this cell. Unfortunately, a number of foundries lack this "skip-a-cell" feature in the release flow. As a result, either the release team must release the design without the necessary design-marking layers, or it must bypass the automation in favor of manual processing.

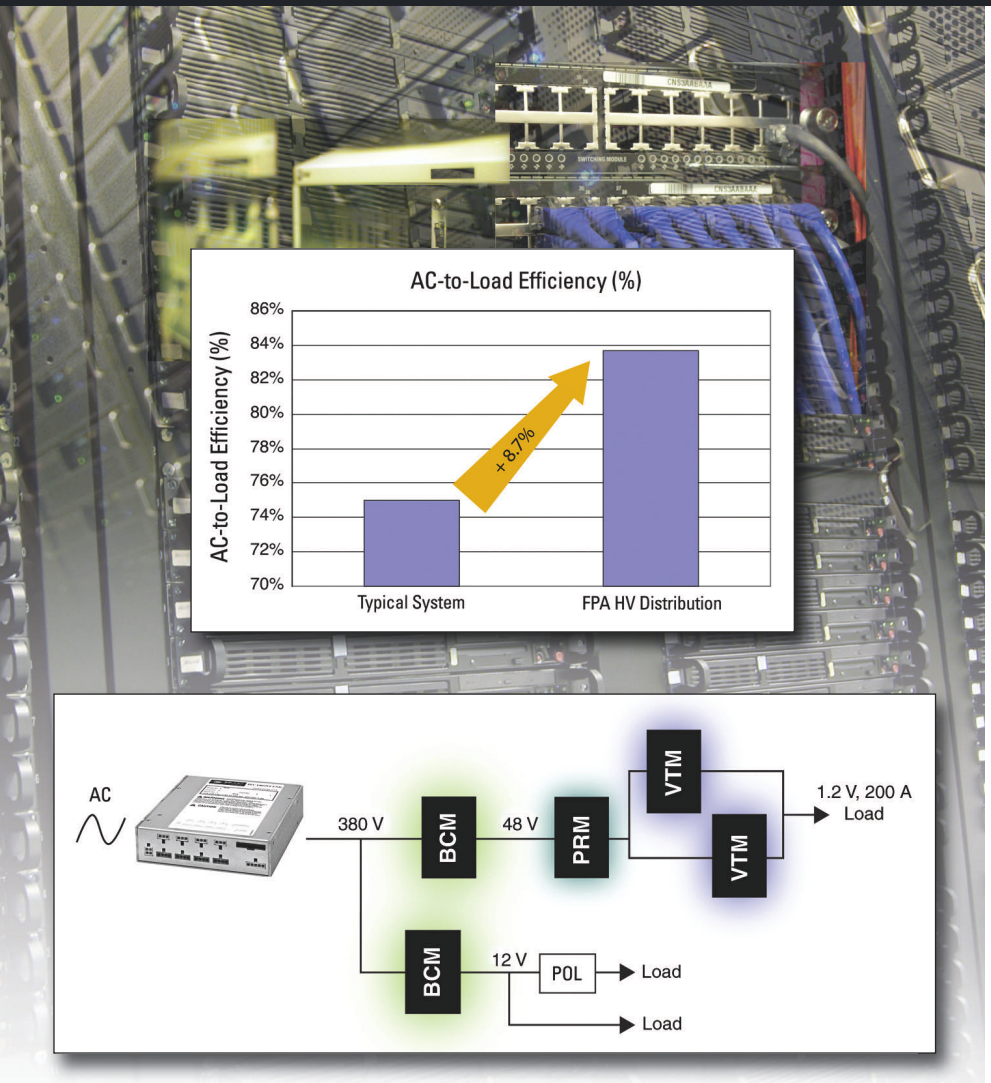
Transferring the design data to the manufacturing facility can itself be a challenge. To transfer this data, designers typically use GDSII (Graphic Design System II), also known as stream data, and Oasis, which are both binary-file formats. Another means of transfer, CIF (common intermediate format), is a popular academic-edition and free EDA tool in ASCII (American Standard Code for Information Interchange) format. To reduce cycle time, physical media is no longer the method of choice. Rather, teams electronically transfer the designs. In the past, these electronic transfers have been in the form of e-mail attachments, but, with new designs having 10s of gigabytes, this method is impractical for most e-mail tools. Smaller designs—typically, CIF designs—can still use e-mail formats, in which you embed the design data in the e-mail body itself. This limitation makes FTP (file-transfer protocol) the protocol of choice. With FTP, the customer can drop the design into a designated secure FTP site at the foundry, or the designer can park the data at the customer site in a secure FTP location for a foundry autobot to collect.

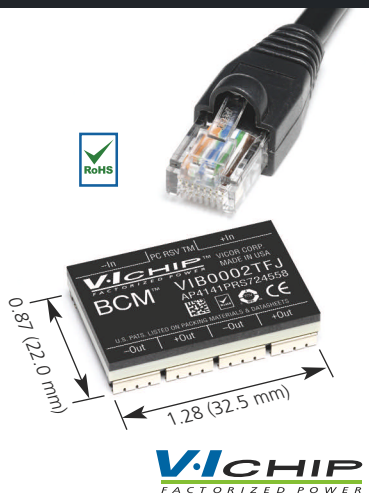
In either case, most networks include significant security provisions that restrict or purposely corrupt the binary data to ensure security and avoid malicious attacks on the network. So design transfer is no longer an engineering task but a collaborative effort in which the involvement of the IT (information-technology) department is an absolute requirement. EDN

Contact me at pallabc@siliconmap.net.

All of the Savings
None of the Loss

HV Bus Converters Enable AC-to-Load Efficiency Increase of 8.7%





V·I CHIP
FACTORIZED POWER

- **High power density: Up to 1120 W/in³**
- **380 V to 1.2 V, 200 A conversion in 4.5 in²**
- **Low noise ZVS – ZCS MHz switching**
- **>95% efficiency**

For high power computing and telecom systems, HV BCM™ bus converters are high efficiency, low noise, high power density system building blocks that enable the highest possible distribution efficiency.

As part of a Factorized Power Architecture solution, the HV BCMs efficiently power sub 1.0 V processor and memory arrays while providing 12 V for disk drives and legacy loads.

To order call
1-800-735-6200 or email
custserv@vicorpower.com

BCM Model No.	Input Voltage (V)		Output Voltage (V)		Output Power (W)	Output Current (A)
	Nom	Range	Nom	Range		
VIB0002TFJ	380	360 – 400	48	45.00 – 50.00	325	7.0
B384F120T30	380	360 - 400	12	11.25 – 12.50	300	25.0
VIB0003TFJ	350	330 – 365	44	41.25 – 45.60	325	7.7
VIB0001TFJ	350	330 - 365	11	10.30 – 11.40	300	28.0

Products in mass production and available from stock

800-735-6200 **vicorpower.com/hvbcm/edn** VICOR

FPGAs CAN BE GREAT AT VIDEO PROCESSING, BUT VERIFYING FPGA-BASED VIDEO SYSTEMS REQUIRES CAREFUL ATTENTION TO YOUR APPROACH.

FPGA VERIFICATION in embedded video-processing systems

BY HARSHAL CHHAYA AND TARAK PATEL • eINFOCHIPS

Participating in the consumer-electronics segment has many advantages. Despite that fact, design teams in this segment will encounter a drastically reduced time-to-market window. Consequently, FPGA (field-programmable-gate-array)-based designs have evolved as the first choice of many system architects. Meanwhile, the increasing requirement for multimedia in consumer products has made DSPs and streaming interfaces must-have components in many embedded products. Several FPGA vendors have developed FPGAs with DSP cores and streaming interfaces that are technologically sufficient and complex enough to handle these recent design requirements.

An FPGA interfacing with DSP cores and with high-speed-video data streaming through it is far from a simple system, however. This increased design complexity has added verification challenges and raised the specter of costly re-spins of the system board if you catch a critical error late in the design cycle. To put that ghost back to bed, you must carefully consider your approach to verification so that you can reduce the risk of costly re-spins.

The largest advantage of FPGA-based design verification is that, at the lowest level, the system has a predefined archi-

tecture, so you know the scope of necessary test scenarios at the beginning of the design. With this fact in mind, a verification team can build on the FPGA a verification environment that mimics the actual system architecture.

In addition to verifying your external peripherals, you must verify any design elements internal to the FPGA, such as the DCM (digital-clock manager) and block RAM, that you use in your designs. This requirement gives you a lot to verify, however. So the time it takes for test cases to complete greatly affects overall product-development time. Therefore, the verification environment must be time-efficient. The early design of a proper verification environment that you develop with an understanding of the FPGA-design elements and external surrounding devices leads to accurate test-case writing and board bring-up.

CORRECT USE OF PRIMITIVES

FPGA vendors provide well-verified FPGA primitives, such as DCM and block RAM. You must comply with certain guidelines to correctly use these primitives in any FPGA design, however. It is crucial to catch any incorrect usage before the design goes to silicon. For example, one such DCM constraint is the allowed clock jitter on the input clock. In a test case, the DCM has a constraint of ±300 psec on cycle jitter when in low-frequency mode. As per design specifications, the input clock for the DCM can be 16.384, 22.5792, or 24.576 MHz. However, during design verification, the DCM unlocks when experimenters switch the input clock from one frequency to the other because switching the frequency inherently violates the input-clock-jitter constraint. So a modified design implements a mechanism to reset the DCM while changing the input-clock frequency. If you do not catch such bugs during the front-end verification, it could easily take a week or more just to identify the bug during board bring-up.

With the advances in technology, FPGAs now include block RAM, which can be either a single- or a dual-port memory. As a dual-port RAM, the block RAM allows both ports to simultaneously access the same memory cell. If the designers improperly implement the RAM controller, however, both memory ports may attempt to write different data to the same RAM location during the same valid write cycle. The verification team must have separate tests for such scenarios. Thus, it is essential that not only a FPGA designer but also a FPGA-verification engineer be aware of the requirements or constraints of internal FPGA components.

AT A GLANCE

- FPGAs can fit the needs of today's video-processing systems.
- In video-processing applications, a lot of care has to go into test-bench design.
- Making the verification environment as similar as possible to the real world eases board-level integration and reduces the need for re-spins.

INPUT-SIGNAL VARIATIONS

In the real world, the input signals to your FPGA have routing-path delays and quality degradations. Your FPGA-verification plan should take into account such variations in timing and signal integrity when generating the input-stimulus signals. It is a good practice, for instance, to know how much drift an input signal would have from an ideal condition so that you can verify that the FPGA design will function smoothly during drift. This requirement becomes crucial when the interface is synchronous and an external device is driving the clock. The data, control, and clock may all have different delays based on the routing-path delay, clock-to-output delay of the transmitting device, and input-setup time of the receiving device. In high-frequency operation, this constraint may leave a narrow sampling window for the FPGA to capture the input data. In such cases, you should consider such real-time delays when providing stimulus to the FPGA design.

In the real world, input clocks come with jitter and drift variations. Although you can use a DCM to deal with these variations, the DCM has its own limitations in its tolerance of input-clock variations. A verification engineer must know the possible clock variations that can occur in the real system and incorporate the same variations when generating input clocks in the verification environment. Adopting such practices can help to discover the limitations of an FPGA design and implement corrective actions during the early development phase.

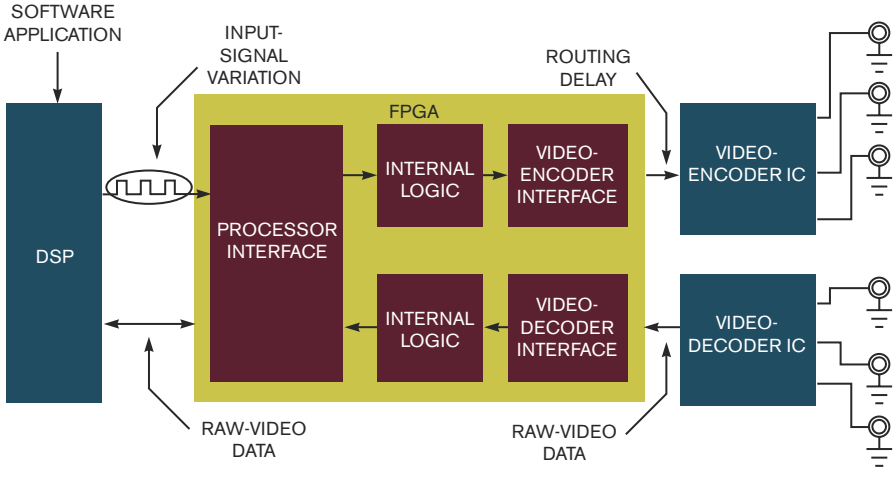


Figure 1 An FPGA can play a central role in a streaming-video application.

PERIPHERAL INTEGRATION

The rapid growth in streaming media requires systems to work at higher speeds. With higher-frequency systems, you must take care when integrating an FPGA with its peripheral devices. Those peripheral devices have timing constraints in input setup-and-hold time. Verification engineers must know these

timing constraints for all the peripheral devices. Adding an oscilloscope for verifying FPGA designs with different timing constraints forces the designers to follow the proper design guidelines to make the FPGA design compatible with the system.

FPGAs may implement standard interfaces, such as UART (universal asynchronous receiver/transmitter), I^2C (inter-integrated circuit), SPI (serial-peripheral interface), and GPIO (general-purpose input/output). The standards should dictate the verification strategy for these ports. When verifying such designs, you must also consider the timing constraints of peripheral devices using custom interfaces. For example, a GPIO interface of an FPGA may interface with an onboard multiplexer. The FPGA is responsible for driving selection inputs of the multiplexer and then capturing the multiplexer output. The multiplexer requires settling time on its outputs once the selection input has changed. Implementing that delay in generating response from a verification model ensures that the FPGA captures the multiplexer output only after the output has settled.

SYNCHRONIZING THE TEAMS

It is a good practice to give the FPGA design under test a feel for the real-time software application flow. FPGA designs that appear to work on the verification testbench may fail to survive when application software imposes some limitations of its own. Consider, for example, an FPGA design for high-definition video capture. The FPGA must capture the raw-video data and fill up an internal FIFO (first-in/first-out) buffer. A DSP, interfacing with the FPGA on its external memory interface, reads the FPGA FIFO buffer to capture the video data (**Figure 1**). Using timing information from the real application-software flow, the verification engineer can estimate the maximum time that the DSP can take between two consecutive FIFO-buffer reads. The engineer can then implement a test case with this DSP limitation in mind. The test records an error if the FIFO buffer is too shallow to buffer all the data that can arrive during the longest interval between two consecutive FIFO-buffer reads.

Problems in video-signal processing can be data-dependent. So it can be important to use different types of video patterns during board bring-up. This approach helps ensure accurate video processing of any video-streaming application. With advances in the open-source community, verification engineers can readily find open-source software to generate such test patterns in raw-data format. Verification engineers can generate such video patterns as a raw-data file using software or by directly capturing patterns from a system (**Figure 2**). Adopting such methods, verification engineers can catch design failures under real-time-test scenarios and fix them during front-end verification itself, not when the customer happens to apply a pattern that breaks the system.

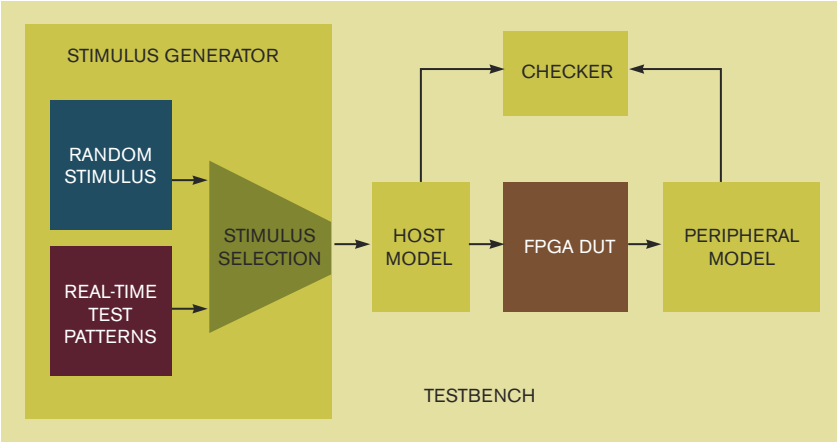


Figure 2 Using software or by capturing patterns directly from a system, verification engineers can catch design failures under real-time-test scenarios and fix them during verification.

Verification and software teams should have a common set of test scenarios in the test plan at the beginning of the design cycle. The common set of test cases would ensure that there are no loopholes during board bring-up. Also, designers can target or rectify any of the implementation or integration errors early in the design cycle.

The complexity of FPGA designs requires designers to detect issues as early as possible in the design cycle to avoid re-spins. The role of verification becomes important in reducing the number of faults arising during board bring-up. Careful consideration of system architecture along with working knowledge of the peripheral hardware will lead verification engineers to write test scenarios closer to the real-time application. These practices can lead to an effective verification effort that will ultimately ease board bring-up. EDN

Go to www.edn.com/090709df and click on Feedback Loop to post a comment on this article.

For more technical articles, go to www.edn.com/features.

AUTHORS' BIOGRAPHIES

Harshal Chhaya is an ASIC engineer at eInfochips, where he has worked for three years. He provides RTL (register-transfer-level) design and verification for FPGAs; SOC (system-on-chip) verification; and IP (intellectual-property) verification, development, and synthesis. Chhaya has a master's degree in electrical engineering from San Jose State University (San Jose, CA). His personal interests include Buddhist philosophy, the education process, and cricket. You can reach him at harshal.chhaya@einfochips.com.

Tarak Patel is an ASIC-verification engineer at eInfochips, where he has worked for three years. He defines and develops verification environments for ASIC and FPGA designs. Patel has a bachelor's degree in electronics and communications from Hemchandracharya North Gujarat University (Gujarat, India). His personal interests include listening to music. You can reach him at tarak.patel@einfochips.com.

Powerful high-level software tools give domain experts in such diverse fields as aerospace engineering, medical electronics, mechatronics, and even graphics design increasing control over the implementation of embedded systems. Such software packages can automatically generate code for target processors or FPGAs, leading to the possibility that dedicated hardware- and software-embedded-system designers may become members of an endangered species. The idea that domain experts might supplant electrical engineers gained wide currency during a 2008 Embedded Systems Conference panel discussion (**Reference 1**). A look at the current state of affairs suggests that domain experts and high-level-system architects—as opposed to coders and processor experts—have gained significant ability to participate throughout the embedded-system-design process. However, the need for C coders and hardware engineers is not going away. In most cases, domain experts and electrical engineers can better collaborate on quickly getting increasingly complex products to market.

ROBOT HAND BY SHADOW ROBOT

HIGH-LEVEL SOFTWARE FOR EMBEDDED-SYSTEM DESIGN DOING YOUR

DOMAIN EXPERTS ARE GAINING MORE CONTROL OF EMBEDDED-SYSTEM DESIGN, BUT ELECTRONIC- AND CODE-DESIGN SKILLS REMAIN KEY TO SUCCESSFUL PROJECTS.

BY RICK NELSON • EDITOR-IN-CHIEF


JOB?!?

"The premise was that people who have to implement an embedded system and the people who know what needs to be implemented never know how to talk to each other," says Jim Tung, a fellow at The MathWorks, commenting on the 2008 panel discussion. "Certainly, the world has moved away from that starting point. What you certainly do see now is collaboration. The people who have the implementation skills … to deliver a device with a certain power consumption and performance profile can work more effectively with the domain experts—the people who know what the performance needs to be." High-level languages, such as The MathWorks' Matlab and Simulink, he says, enable that collaboration to take place.

AT A GLANCE

- In most cases, domain experts and electrical engineers can better collaborate on quickly getting increasingly complex products to market.
- High-level languages, such as The MathWorks' Matlab and Simulink, encourage collaboration between domain experts and engineers.
- National Instruments has moved into the embedded-system-design area, but the company is not moving away from test.
- Automatic code generation has reached the point at which the resulting code is efficient enough in memory and provides sufficient throughput to suffice for many applications.

TEST SOFTWARE

National Instruments has been promoting its LabView graphical-design software, which initially served test-and-measurement applications, as a tool for embedded-system design. "With the thousands of technical challenges the engineering community faces today in applications such as medical, robotics, and 'green,' we don't have enough embedded-engineering experts," says an NI spokeswoman. "Therefore, the masses of domain experts out there become critical parts of helping out the engineering community. We've seen numerous domain experts be very successful using our graphical-system-design tools to design embedded systems in the medical, robotics, and renewable-energy industries, and we will continue creating embedded hardware and software tools that allow any domain experts and scientists to innovate themselves and design embedded systems."

One NI customer that has successfully used NI tools in embedded-system design is Alliance Spacesystems, which makes mechatronics systems, such as robots for NASA (National Aeronautics and Space Administration). Shelley Gretlein, LabView real-time and embedded-product-marketing manager at NI, describes Alliance Spacesystems' mechatronics group as a multidisciplinary team comprising aerospace, mechanical, electrical, and control engineers all cooperating on the same team. "You see much less pure EE [electrical-engineering] or strong embedded experience," she says. "Much more, you see people coming from different backgrounds to build these systems."

The move to the embedded-system area has been an evolutionary one for NI, but that doesn't mean that the company is moving away from test. "Test is NI's bread and butter," says Todd Dobberstein, product manager of industrial and embedded technologies for NI. "We've been dealing with test and data acquisition since we started as a company." The company's test expertise, he says, complements the design capabilities inherent in LabView. At Alliance Spacesystems, NI's Gretlein works with a group that began as a test customer and has increasingly adopted NI tools for design, leading to a unified tool chain.

PJ Tanzillo, biomedical-segment lead and embedded-software manager at NI, cites another customer that has applied NI's tools in an embedded-system-design project: Sanarus successfully designed the Visica 2 cryoablation system for the treatment of tumors (**Figure 1**). Tanzillo describes the system engineer on the project, Jeff Stevens, not as a do-

Figure 1 The Visica 2 cryoablation system for the treatment of tumors (a) went from a requirements document to first revenue in 14 months, according to system engineer Jeff Stevens (courtesy Sanarus). Stevens used LabView to develop code for the CompactRIO platform (b) that served as the embedded engine in Visica 2 (courtesy National Instruments).

main expert but as an electrical engineer by training whose expertise is at the system-architecture level rather than the coding and hardware-optimization level. Such system architects may be able to apply their talent across multiple disciplines from robotics to medical electronics, but, Tanzillo says, they understand the underlying technology, albeit not necessarily down to the level of developing a driver for an ADC or writing HDL (hardware-description-language) code for an FPGA.

DESIGNING THE VISICA 2

Stevens describes himself as a systems engineer with degrees in electrical engineering who thought that any code he had written would never see the light of day. That situation changed, however, when he joined Sanarus in November 2005 as principal system engineer. There, Stevens faced a tough deadline: developing a fully functional prototype of the Visica 2 within four months. "As the system architect, I could see that we'd need a custom PCB [printed-circuit board] for the microprocessor and all the I/O and that we'd have to outsource all the firmware because nobody at Sanarus spoke software," he says. "That was the approach Sanarus had followed on its previous product, but that product was an order of magnitude simpler than Visica 2." Further complicating the task was the fact that the team available to work on the project would be small. Besides Stevens, the team comprised a mechanical engineer; a "supertech," who had a degree in psychology but was creative at prototyping, knew how to run milling machines and lathes, and could solder PCBs; and a project manager. "The joke was that we kept [the manager] out of the lab," Stevens says. "I was thinking eight months might be enough to accommodate board and code spins plus integration, but four months fell squarely in the 'no-way' bucket."

However, he then investigated NI's CompactRIO (reconfigurable-input/output) platform as a hardware target for embedded code that could run software that he could develop on LabView—a tool he had heard of but had never used. Stevens presented his case to Sanarus management and got approval to adopt the NI approach. With the help of NI support personnel and a developer from CalBay Systems, he "comfortably hit the working prototype in the four-month target." He adds, "Visica 2 went from a requirements document to first revenue in 14 months, which is pretty good for an invasive medical device. *The Wall Street Journal* awarded Visica 2 the runner-up prize for medical devices in its 2008 Technology Innovation competition." (**Reference 2**). To support a lower-cost production version of the Visica 2, Stevens ported his code from the CompactRIO platform to Single Board RIO (**Figure 2**). "I got access to Single Board RIO before [NI] publicly announced it," he says. "The porting took about 45 minutes."

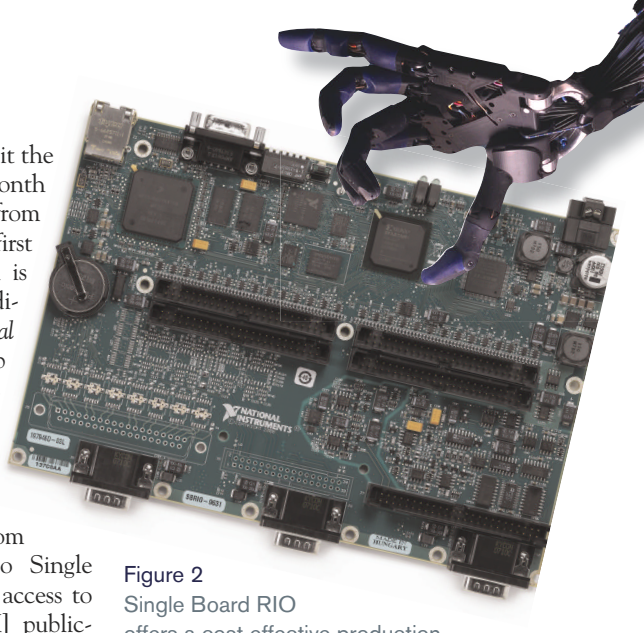


Figure 2
Single Board RIO offers a cost-effective production alternative for CompactRIO prototypes. System engineer Jeff Stevens ported the Visica 2 code from CompactRIO to Single Board RIO in about 45 minutes (courtesy National Instruments).

HIGH-LEVEL ABSTRACTION

Sanarus completed the Visica 2 project without the intervention of traditional embedded-system designers. That situation may be the exception that proves the rule, however. "Think about the 'good old days,'" says The MathWorks' Tung. "If you wanted high-performance software running on your desktop, you had to write in assembler. That's why Lotus 123 was so lean and so fast." Subsequently, "optimizing compilers have reduced the need for people to work at that level, so they are able to work at a higher level of abstraction—say, C code," he adds.

According to Tung, domain experts will want to work at an even higher level of abstraction with Simulink, for example. Automatic code generation has reached the point at which the resulting code is efficient enough in memory and provides sufficient throughput to suffice for many applications. "However, there are still times when you need to really tune and optimize that implementation, so the need in an embedded system for somebody to write in C code hasn't gone away. It just happens less frequently," he says. "If I am gong to write something and really fine-tune it at the C-code level, I want to do that only once. If I'm going to handwrite something, then a high-level modeling language, such as Simulink, should be able to encapsulate it and make it available to the system-level engineers so they can look at the design-exploration trade-offs and make a much more informed decision, and [this approach] facilitates reuse."

Software-development teams would continue to need to consider issues such as when to deploy an RTOS (real-time operating system) and when it would be necessary to consider race conditions and task overruns, Tung says. "I think it's simplistic to say that the development team can ignore those issues on a forward-going basis. It's not really a question of whether the domain expert will ever be able to automatically just push a button and have a beautiful, efficient embedded system," he explains. "It's more of a question of, Can a design team quickly look at the various ways of implementing a system that addresses the domain issues but also addresses the implementation issues, and get it done in as streamlined a fashion as possible?"

FLOATING VERSUS FIXED

When Sanarus' Stevens got started on the Visica 2 project, he knew that his hardware target was CompactRIO. Often, however, system architects and domain experts don't know what target embedded software will ultimately run on. Tung explains that a system engineer working in Matlab might describe an algorithm in floating-point terms, but that algorithm might ultimately run on a fixed-point processor. "You are not going to just put the algorithm on the fixed-point processor and assume it's

Figure 3 One of two BA609 tilt-rotor aircraft undergoes flight testing, flying in airplane mode over the Alps in northern Italy (courtesy Bell/Agusta Aerospace Co).

going to work," he says. "Over the last five years or more, [we've] enabled the persons working in Matlab or Simulink to essentially say within that environment that they are going to work on a 16-bit processor" so that they evaluate the behavior of their algorithm as it will work on that fixed-point processor. "A person working 10 years ago in an ideal algorithm would find all kinds of late surprises," Tung adds. "By being able to evaluate the fixed-point performance in the Matlab or Simulink environment, the domain expert is able to look at the implementation effects and determine the impact."

DOMAINS VERSUS SYSTEMS

Like NI's Tanzillo, Tung distinguishes between domain experts and system engineers or architects. Although NI promotes LabView for both, Tung says that domain experts working at the algorithmic level more often use Matlab, whereas an increasing number of Simulink users are "multidomain in their perspective." He cites a mechatronics example, in which a system includes mechanical, electronic, and embedded-software components. "The system-level view needs to capture each of those domains to let the system-level engineer say, 'Is that design going to meet my requirements?' The engineer would then ask, 'If I needed to tune something in a domain to achieve the system-level performance I need, should I tune it in the embedded software, by changing the mechanical design, or by changing electronic design?' And the nice thing about the Simulink environment," Tung says, "is that the persons working with the Simulink models are able to look at the system design from any or all of those domain perspectives, and they are able to make changes in one of the domains and perhaps loosen up the requirements in another domain. The Simulink environment traverses the gap … between the person who is thinking about things from an algorithmic standpoint and the person who thinks about it from an implementation standpoint."

Tung also notes that, apart from performing system design, users of high-level tools can leverage them to perform verification. "Let's take a case in automotive-suspension systems," he says. "You'll have the model of the suspension systems and the algorithms that will be describing the damping and other behaviors, but you will also have the portion of the models that will be describing road surfaces, vehicle dynamics, driver behavior, and all the other things important to understanding if the suspension will do what you want. One portion of the models that describes the suspension system can automatically generate the code that goes into the microcontroller, and it ships as part of the car. The other portion of the models … becomes the basis for the test bed; you essentially generate code for that other portion of the model comprising the road surface, the vehicle dynamics, and the driver, and you run that [code] in a real-time HIL [hardware-in-the-loop] system that essentially is the test bed."

FLY BY WIRE AT BELL/AGUSTA

David King, principal engineer at Bell/Agusta Aerospace Co, also has opinions on trends with domain experts. "Look-

ing back 15 years when we did some of our legacy fly-by-wire development programs, we had a much larger proportion of specialists for low-level programming languages on our team," he says. "Now, if we look at the proportion of the team, the majority of them are not well-versed in the low-level languages, but they are more or less system-level engineers using the model-based design process." The shift seems to be gradual, he adds. "I don't see that we are dropping our number of specialists in the programming languages, but we are growing on the systems side, so the proportion is changing," bringing good news for embedded-system designers.

King is currently working on the Bell/Agusta BA609 aircraft project, the first commercial, nine-passenger, tilt-rotor vehicle (**Figure 3**). The 609 program provides some perspective. "We started with model-based design in 1998," he says. "That was even before the term 'model-based design' was coined. We put together a process using Matlab and Simulink to try to take out some of the manual steps in the process, such as hand-coding from design data. And the one thing that's interesting is it's not just hand-coding for the embedded source code, but it was the hand-coding for all the analytical tools that analyze the various aspects of the aircraft and system performance," including simulation, development of the test cases, and verification.

Bell still employs hand-coded embedded software in the flight-control computers on the aircraft but uses the auto-coded models for all the analytical tools to perform simulation, structural analysis, stability analysis, and test-case generation, all of which, King says, represent a big chunk of the workload. "I am really seeing the benefit of model-based design in that we can have one model of the aircraft and the flight-control system that is in a very usable format, and that model is used by various disciplines to do analysis." He adds, "For example, we use it for simulation to analyze dynamic loads and to analyze handling qualities. We use it for real-time simulation with the pilot in the loop, and we also use it for non-real-time evaluation when we are checking stability and control characteristics."

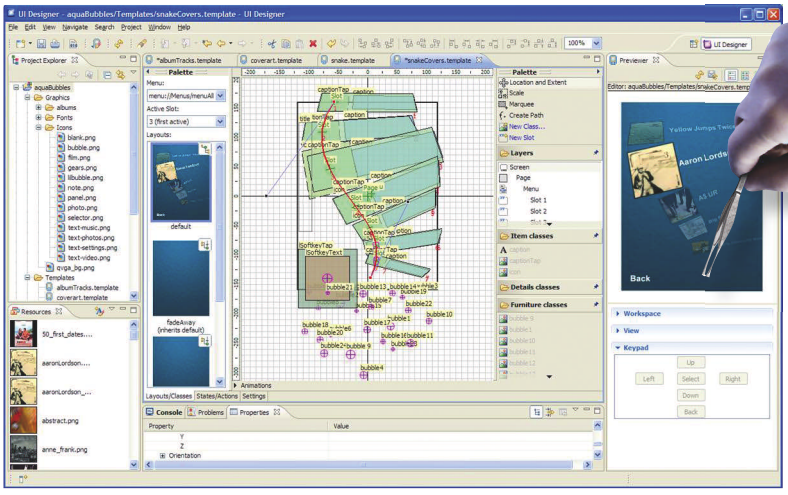


Figure 4 Domain experts—in this case, creative and usability specialists—can now contribute directly to the development of embedded products' user interfaces by employing the drag-and-drop Nucleus Graphics Designer tool (courtesy Mentor Graphics).

In addition, the use of standard models in Matlab and Simulink makes it easier to work with partners, including the company that builds the flight computers, and eases certification. Now, one aircraft in Texas and one in Italy are undergoing flight testing, which is about 75% complete, in anticipation of the beginning of the certification process with the FAA (Federal Aviation Administration) and the European Aviation Safety Agency. The Simulink pages become part of the software-design data for the FAA-mandated DO-178B design-assurance process for the software development. King expects the trend to continue toward an increasing emphasis on high-level tools. "If you look at the tool set and the maturity of the tools that The MathWorks produces and that the industry is using now, they've progressed quite a bit since we started [the 609] program 11 years ago," he says. "For our next programs, we are looking at additional automated steps, including [generating the] embedded software."

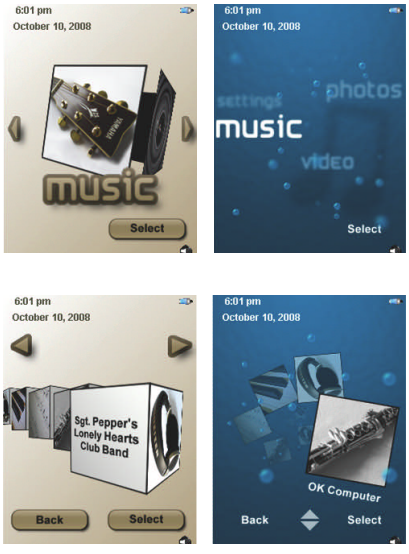


Figure 5 Artists have created two user interfaces with no coding or scripting using the drag-and-drop Nucleus Graphics Designer tool (courtesy Mentor Graphics).

PRODUCT DIFFERENTIATION

Mentor Graphics addresses the embedded-system market with several product lines, including the Nucleus RTOS, which, according to Geoff Kendall, product-marketing manager for the embedded-systems division at Mentor, is the most widely deployed commercial RTOS because of its penetration in the mobile-phone market. When it comes to domain expertise, however, the relevant tool is the Nucleus Graphics embedded UI (user-interface) engine and designer tool, and the relevant domain experts are graphics artists (**figures 4** and **5**). Kendall calls the Nucleus Graphics Designer tool a "framework that allows you to completely separate the de-

sign and presentation of the user interface from the functions underneath it." He describes the traditional design flow: "For example, you've got graphic designers who mock up concepts in Photoshop to show what the screen should look like [with respect to menus and so forth]. The way it has traditionally worked, a couple of guys sit there coming up with those concepts; then they hand them over to the engineers, and the engineers roll their eyes and say, 'We'll do our best, but we've got a bit of a crunch on.' And you end up with a product that may be off to market on time and maybe slightly resembles what the graphic designers wanted, but it is probably not ideal for everyone.

"The domain experts here," Kendall continues, "are the usability experts—in this case, the guys who know how to make a product work well and differentiate it from the other products on the shelf. But they are not the guys who really understand how to push pixels around the screen with an embedded processor." One approach is to run a program that the graphics designers understand, such as Adobe Flash, on the target device. "Anyone who has tried to do that [task] will tell you Flash was never designed for the performance constraints of an embedded platform," he says. "The exact attributes of Flash that made it so powerful and so dominant in the world of PCs and Web browsers are actual liabilities in the embedded space. For example, the reliance of Flash on vector graphics allows it to display on any screen size very well on a desktop PC, but that [ability] actually requires a lot more processing power to be able to render graphics in real time. So when you get down to an embedded device with a constrained screen size, you still have the computational hit of rendering those vector graphics. You actually start to see a significant performance falloff to the point that, if you use a native-UI technology like ours, you could be getting 15 or 20 frames of animation a second even on an ARM7 device. You would barely even get Flash running on that device at one or two frames per second."

The Mentor Nucleus Graphics Designer tool, Kendall says, "allows people with no programming or even any scripting [experience] to be able to drag and drop their UI designs to completely change and define the look and feel of a device, and they can do that in parallel with the engineers working on the coding with no interdependencies between the two whatsoever."

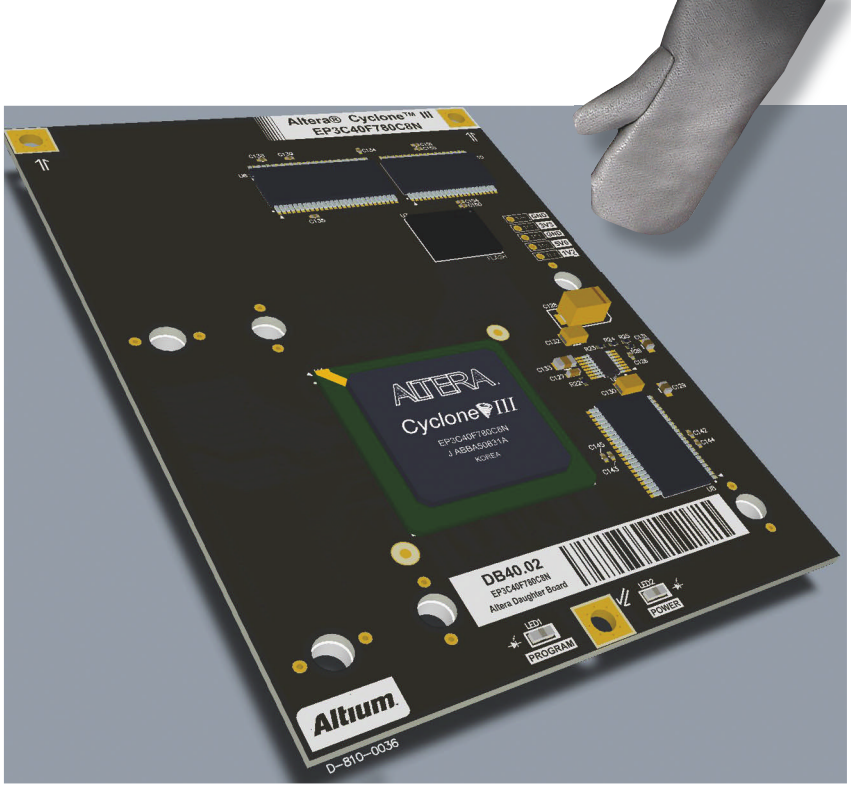


Figure 6 In conjunction with the Altium Designer unified-electronics-design tool, this daughterboard for its desktop NanoBoard reconfigurable-hardware-development platform targets Altera's Cyclone III EP3C40 FPGA in a 780-bump BGA package (courtesy Altium).

With respect to product differentiation, he adds, the tool is "particularly relevant for guys who are building embedded products that will have multiple end customers. Imagine, for example, an in-car-entertainment system that a company is building for use by multiple automobile manufacturers, such as Ford, Daimler, and Ferrari." These customers want different user experiences, but the supplier ideally wants one code base that never changes. The designer tool, says Kendall, supports that requirement without any recompilation of code.

Go to www.edn.com/090709cs and click on Feedback Loop to post a comment on this article.

For more technical articles, go to www.edn.com/features.

The concept extends far beyond automotive applications. "A number of big vendors of white goods actually have multiple consumer-facing brands," Kendall explains, "and they need to make products that will look different for each of those brands. If they are doing that [task] by having different-shaped plastic dials and buttons, then it gets pretty expensive to do, and, if they start adding more features, they've got more and more buttons to add. It gets to the point where it actually becomes more cost-effective to start adding a screen to these devices. And we are now starting to see the likes of Samsung and Sony and big consumer-electronics companies starting to add touchscreen UIs even to things like fridges." Mentor is well-positioned, he says, to support the "demand for adding interactive-touchscreen capability to devices that, two or three years ago, you would never have considered would need it."

Tools such as Nucleus Graphics Designer are becoming more important as silicon becomes more complex. A lot of today's processors that are going into devices with screens offer features such as Open GL 3-D hardware acceleration.

"This is all great stuff," says Kendall. "But unless you've got software on top of it that lets you unlock the power, it's just wasting space." The designer tool doesn't require hardware features, such as acceleration, but takes advantage of them if they are there, he explains. "It will allow the graphic designer to be able to do things like spin stuff onto the screen, fade it away—the kind of effects you'd normally expect to see in top TV production." There has been a technical gap between what the graphic designers wanted to do and what the engineers had the time and experience to be able to build and deliver. The designer tool provides a layer of abstraction over the complex silicon to enable drag-and-drop graphical design to bridge that gap.

CONTINUED EVOLUTION

Marty Hauff, master electronics-designer-success manager at Altium, expects to see continued evolution in the role of domain experts. His company supports the system-design process with its Altium Designer software for FPGA-populated PCBs; the company also offers related development boards (**Figure 6**). "As design abstraction increases, low-level hardware/software/microprocessor skills will become less important," he says. "Innovation will move out of the hardware/software-design process and move into the overall user experience. A system-level designer could then be responsible for the specification and innovation of a system, and the low-level stuff would be farmed out as necessary." Hauff likens what is happening in the embedded-system market to what has happened in the PC arena. "With tools such as VBA [Visual Basic for Applications] being embedded into Microsoft Office apps, nontraditional programmers can now create very advanced applications without needing to know too much about the underlying hardware," he says. "And, with Web-based languages, such as Java and C#, software developers can now build applications with zero knowledge of the underlying hardware."

Hauff doesn't write off dedicated embedded-systems engineers, however: "I think it is probably a little too strong to say that domain experts will supplant engineers. I would argue that a design role is still required, but the skill necessary to fulfill that role will change. So it may well be that the nature of what engineers do changes. The need for low-level design engineers may be replaced by a greater need for system-level-integration engineers, and so on. This [scenario] is consistent with what has happened to engineers in the past. As ICs have packed more functions, engineers can operate at a higher level of abstraction and create new products without needing to know as much low-level detail."EDN

FOR MORE INFORMATION

Adobe
www.adobe.com

Alliance Spacesystems
www.alliancespacesystems.com

Altera
www.altera.com

Altium
www.altium.com

ARM
www.arm.com

Bell/Agusta Aerospace Co
www.bellagusta.com

Cal-Bay Systems
www.calbay.com

Embedded Systems Conference
www.embedded.com

The MathWorks
www.mathworks.com

Mentor Graphics
www.mentor.com

Microsoft
www.microsoft.com

National Aeronautics and Space Administration
www.nasa.gov

National Instruments
www.ni.com

OpenGL
www.opengl.org

Samsung
www.samsung.com

Sanarus
www.sanarus.com

Sony
www.sony.com

REFERENCES

1 Nelson, Rick, "Engineers to be supplanted by domain experts?" *Test & Measurement World*, April 21, 2008, www.tmworld.com/blog/640000064/post/280025228.html.

2 Totty, Michael, "The 2008 Technology Innovation Awards," *The Wall Street Journal*, Sept 29, 2008, http://online.wsj.com/article/SB122227003788371453.html.

BY ROBERTO MATTIUZZO AND DAVIDE APPELLO, STMICROELECTRONICS • CHRIS ALLSUP, SYNOPSYS

SDD AUTOMATIC-TEST-PATTERN GENERATION BREAKS THE NANOMETER-QUALITY BARRIER.

SMALL-DELAY-DEFECT TESTING

Semiconductor companies have come to rely on delay testing to attain high defect coverage of manufactured digital ICs. Delay testing uses TD (transition-delay) patterns that ATPG (automatic-test-pattern-generation) tools create to target subtle manufacturing defects in fabricated designs. Although TD ATPG improves defect coverage beyond the levels that stuck-at patterns alone can achieve, the method is limited in its ability to reach the test-quality levels that nanometer designs require. As a result, STMicroelectronics is deploying SDD (small-delay-defect) ATPG as a means of achieving even higher defect coverage than standard TD ATPG.

WHY SDDs?

"Delay defect" refers to any type of physical defect or an interaction of defects that adds enough signal-propagation delay in a device to produce an invalid response when the device operates at the targeted frequency. Experimental data going back two decades have shown that the distribution of delay-related failures is skewed toward the smaller delays (**references 1** and **2**). That is, most devices that fail due to delay defects fail because of SDDs that contribute to delays much smaller than the clock-cycle times associated with the process-technology node. Targeting these SDDs during testing improves defect coverage and lowers the test-escape rate, measured as DPPM (defective parts per million).

On-chip process variations are more pronounced in today's manufacturing processes because of the increased pres-

ence of systematic defects—stemming from complex interactions between layout, mask manufacturing, and wafer processing—compared with previous process technologies (**Reference 3**). These process variations tend to further skew the delay-failure distribution toward smaller delays, adding enough incremental signal delay to adversely affect circuit timing in a higher percentage of devices. In essence, for a given die size, the product yield of a 45-nm design can decrease sufficiently over that of a 90-nm design that manufacturers must boost the coverage of SDDs just to maintain about the same DPPM levels as those for the 90-nm process.

AT A GLANCE

- Although TD (transition-delay) ATPG (automatic-test-pattern generation) improves defect coverage beyond the levels that stuck-at patterns alone can achieve, the method is limited in its ability to reach the test-quality levels that nanometer designs require.
- To minimize runtime and pattern count, TD ATPG uses a low-hanging-fruit approach to targeting TD faults—along the easiest sensitization and detection paths it can find.
- SDD (small-delay-defect) testing is feasible only if the ATPG tool can make efficient decisions—often thousands per pattern.
- SDD ATPG will be essential to achieving very high defect coverage levels in the years ahead.

LIMITATION OF TD TESTING

So, why doesn't standard TD testing cover SDDs? In fact, it does cover some of them, but not enough to achieve the necessary quality levels for STMicroelectronics, which is pursuing a strategic quality objective of zero DPPM.

The traditional goal of ATPG tools has been to minimize runtime and pattern count, not to cover SDDs. TD ATPG targets delay defects by generating one pattern to launch a transition through a delay fault site—which may activate either a slow-to-rise or a slow-to-fall defect—and by generating a second pattern to capture the response. During testing, if the signal doesn't propagate to an endpoint—that is, a primary output or scan flop—in the at-speed cycle time, then the test captures incorrect data. In this scenario, the pattern sequence detects a delay defect through the activated path.

To minimize runtime and pattern count, TD ATPG uses a low-hanging-fruit approach to targeting TD faults: It targets them along the easiest—and, usually, the shortest—sensitization and detection paths it can find. To understand how this approach affects SDD coverage, consider the circuit in **Figure 1,** which shows three possible detection paths for a single delay fault. TD ATPG typically generates a pattern sequence that targets the fault along the path that has the largest timing slack, Path 3. Note that this pattern sequence doesn't cover SDDs associated with Paths 1 and 2 that targeting the path with smallest slack, Path 1, would have covered.

TD ATPG does manage, however, to detect some SDDs, either directly as targeted faults or indirectly as bonus faults when targeting other faults. Even so, TD ATPG rarely detects delay faults along the longest paths that are necessary to detect the smallest defects—that is, those with the smallest delay. TD ATPG is effective for detecting nominal and large delay defects, but, because it doesn't explicitly target delay faults along the minimum-slack paths, it's ineffective in detecting relatively small delay defects.

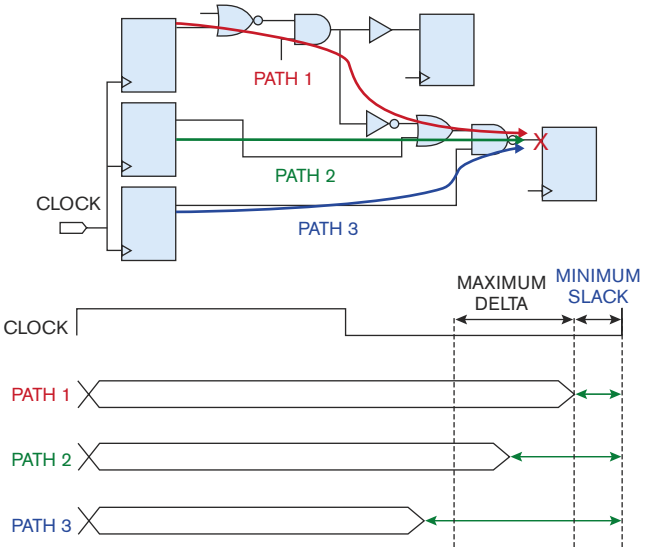


Figure 1 Coverage of small-delay defects depends on the fault's path of detection and the amount of slack in that path (green arrows). Path 1 exhibits the minimum slack.

SDD ATPG

In its purest form, SDD ATPG is similar to path-delay testing. It targets each undetected fault along the path with minimum timing slack. In **Figure 1**, Path 1 has the minimum slack, so the pattern generator targets the fault through Path 1. If the pattern generator detects the fault, it categorizes it as DS (detected by simulation). The fault simulator also classifies bonus faults as DS if it detects them along their minimum-slack paths.

If the test detects a targeted fault or a bonus fault along a path shorter than its minimum-slack path, it designates it as TP (transition partially detected). ATPG continues to simulate TP faults each time it generates a new pattern in the hope that a pattern will eventually emerge that detects, as a bonus fault, this same fault through its minimum-slack path. The main drawback of this method is that, in targeting every undetected fault along its minimum-slack path, SDD ATPG wastes time and patterns working on faults that don't contribute to detecting SDDs.

To illustrate, **Figure 2** represents the histogram of all TD faults in a hypothetical design, with the faults normally distributed according to their minimum slacks. For each discrete value of slack, a certain number of faults in the design have this value as their minimum slack. There are nearly 15,000 faults in the design with minimum slack of 0.5 nsec. Some 200,000 faults, or 20% of the total, have minimum slack less than or

equal to 0.5 nsec. Targeting faults with minimum slack in this lower range is an effective way to test for SDDs. On the other hand, targeting faults with much higher minimum slacks doesn't detect SDDs; the slacks of these faults are large enough that standard TD ATPG efficiently covers them.

A hybrid approach to pattern generation uses SDD ATPG to target faults having relatively small minimum slack along their minimum-slack paths and uses TD ATPG to target the remaining faults along their easiest-to-detect paths. Synopsys' TetraMax ATPG product uses the maximum-timing-margin parameter to assign the cutoff-slack level for targeting faults at their minimum slacks (**Reference 4**). SDD-ATPG algorithms target faults along paths with minimum slack less than or equal to the maximum-timing-margin parameter, and TD-ATPG algorithms target other faults.

When the minimum slack of a detected fault exceeds the maximum timing margin, the fault is TP even if the algorithm detects the fault along its minimum-slack path. Narrowing the scope of SDD ATPG to focus on what it does best—testing for SDDs—significantly reduces both pattern count and runtime.

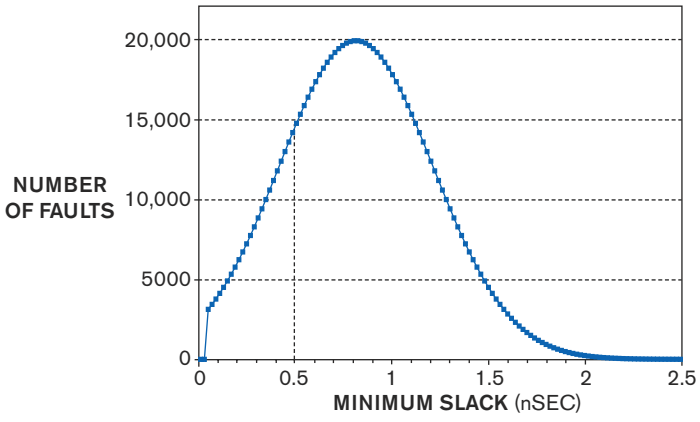


Figure 2 For each discrete value of slack, a certain number of transition-delay faults in the design have this value as their minimum slack.

REDUCING PATTERN COUNT

In some situations, it may be beneficial to further reduce the pattern count of SDD ATPG. One approach is to let ATPG generate a pattern that can still detect small—though not always the smallest—delay defects related to a fault. TetraMax ATPG uses the maximum-delta parameter to control this behavior. If the slack of the detection path for a fault exceeds the fault's minimum slack by not more than the value of the maximum-delta parameter, then the fault simulator classifies the fault as DS.

If ATPG cannot detect the targeted fault through its minimum-slack path, it will attempt to target the same fault through a path with larger slack (**Figure 1**). The slack of Path 2 is less than the sum of the fault's minimum slack and the value of maximum delta, so detecting the fault along Path 2 causes the fault simulator to classify the fault as DS. The slack of Path 3, however, exceeds the minimum slack of the fault plus the value of maximum delta, so detecting the fault along this shorter path causes the fault simulator to classify the fault as TP.

Increasing maximum delta above its default value of zero reduces pattern count because more faults per pattern pass the criterion for DS classification and fewer faults need to be targeted by ATPG in each subsequent pattern. Moreover, with each succeeding generated pattern, there are fewer TP faults for the fault simulator to

MINIMUM SLACK

DELTA	0.04	0.06	0.08	0.10	0.12	0.14	0.16	0.18	0.20	0.22	0.24	0.26	0.28	0.30	0.32	0.34	0.36	0.38	0.40	0.42	0.44	0.46	0.48	0.50	0.52	0.54	0.56	0.58	0.60
0.00	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP	TP
0.02	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP
0.04	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP
0.06	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP
0.08	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP
0.10	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP
0.12	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP
0.14	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP
0.16	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP
0.18	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP
0.20	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP
0.22	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP
0.24	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP
0.26	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP
0.28	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP
0.30	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	DS	TP	TP	TP	TP
0.32	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.34	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.36	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.38	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.40	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.42	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.44	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.46	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.48	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.50	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.52	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.54	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.56	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.58	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP
0.60	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP	TP

Figure 3 A detected fault contributes to delay effectiveness depending on the ATPG parameters maximum timing margin and maximum delta and the slack of the detection path. In this example, maximum timing margin is 0.5 nsec and maximum delta is 0.3 nsec. The fault is a DS or a TP fault depending on the fault's minimum slack, the additional slack needed to detect the fault (delta), and the ATPG parameters. The red-shaded combinations contribute to delay effectiveness.

track, so the simulation runtime decreases. A nonzero value of maximum delta, however, reduces delay effectiveness.

DELAY EFFECTIVENESS

Delay effectiveness quantifies how successfully patterns detect faults through their longest paths. Only faults that are detected along paths having slacks less than or equal to the maximum-timing-margin parameter contribute to delay effectiveness. These faults can include both DS and TP faults. TP faults can contribute to delay effectiveness because ATPG could detect a fault along a path with slack less than the maximum-timing-margin parameter, even though the slack exceeds the minimum slack of the fault plus the value of maximum delta.

Figure 3 illustrates how a detected fault can contribute to delay effectiveness depending on the slack of its detection path and the maximum-timing-margin and maximum-delta parameters, which are 0.5 and 0.3 nsec, respectively, in this example. The slack of the detection path is simply the sum of the minimum slack of the fault and the additional slack needed to detect the fault, or delta.

The entry for each combination of minimum slack and delta indicates whether the detected fault is of type DS or TP, with red-shaded entries representing those combinations that result in the fault's contributing to delay effectiveness. The **sidebar** "Test effectiveness" describes test coverage and delay effectiveness calculations for SDD testing, as well as how the maximum timing margin and maximum delta affect these metrics.

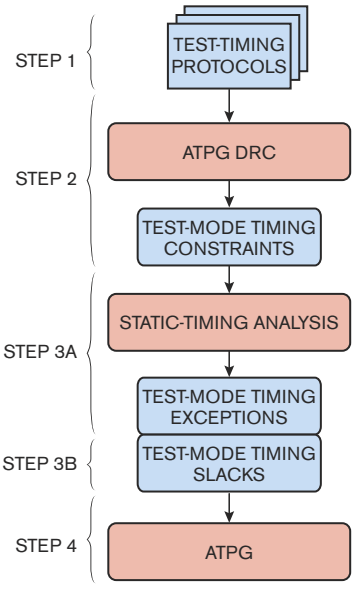


Figure 4 The flow for generating slack data and timing-exception data for SDD ATPG involves a four-step process.

TIMING IS EVERYTHING

SDD testing is feasible only if the ATPG tool can make efficient decisions—often thousands per pattern—using accurate timing information about the design. However, the need to dynamically perform timing calculations inside the ATPG tool, based on Standard Delay Format data, for example, compromises runtime performance and can produce results that don't correlate well with sign-off timing analysis.

TetraMax ATPG avoids these issues by accessing data that Synopsys' PrimeTime static-timing-analysis tool generates. PrimeTime models all the key process, physical, noise, and clock-network effects necessary for accurate timing analysis of nanometer designs, so it helps TetraMax ATPG target SDDs.

SDD ATPG requires two basic kinds of timing information: slack data and timing-exception data. **Figure 4** depicts the four-step flow for generating this information. First, the STIL (Standard Test Interface Language) SPF (STIL-procedure file) describes the test-mode protocols for launch and capture. The TetraMax ATPG DRC (design-rule checker) then interprets the launch-and-capture timing requirements and produces an SDC (Synopsys Design Constraints) file that defines the launch- and capture-mode timing constraints. PrimeTime interprets the launch- and capture-mode timing constraints and produces an SDC file that defines the test-mode timing exceptions. It also generates a report containing the test-mode timing slacks for each fault site. TetraMax ATPG then reads in the slack and timing-exception information that PrimeTime produces to generate SDD patterns.

The correct processing of timing exceptions is essential to both SDD ATPG and standard TD ATPG; the combined flow for SDD testing differs only in the requirement for importing slack data from PrimeTime to TetraMax ATPG (step 3B of **Figure 4**). The flow ensures that the design's timing constraints reflect the test-mode launch-and-capture timing, which differs fundamentally from mission-mode timing.

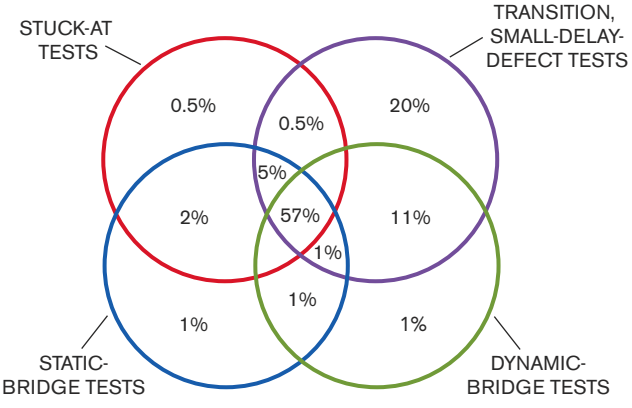


Figure 5 STMicroelectronics collected data from stuck-at, static-bridging, dynamic-bridging, and delay tests. The numbers indicate the percentage of failing parts covered by each type of test.

SILICON-TESTING RESULTS

STMicroelectronics considers SDD testing key to reducing DPPM levels across the company's product lines. As a result, STMicroelectronics now supports the Synopsys flow for SDD pattern generation in its sign-off methodology. The company finds that SDD testing improves test quality over standard TD testing or any other type of test in use today. Evidence for this finding comes from failure statistics STMicroelectronics collected for an automotive IC that it designed and manufactured. The company manu-

factured the design, comprising approximately 1 million equivalent gates, in a 90-nm-CMOS process.

STMicroelectronics collected data from testing hundreds of thousands of parts using stuck-at, static-bridging, dynamic-bridging, and delay tests (**Figure 5**). The delay tests comprised standard TD and SDD patterns. The data indicate that the delay tests covered approximately 94.5% of all failing parts and that 20% of the failing parts were covered only by the delay tests.

Upon examining the data for the 20% of defective parts covered only by the delay tests, STMicroelectronics observed that 64% of these parts were covered only by the SDD patterns. SDD patterns covered the remaining 37% that TD patterns also covered. Test engineers at the company have observed results simi-

TEST EFFECTIVENESS

SDD (small-delay-defect) ATPG (automatic-test-pattern generation) produces two distinct coverage metrics–test coverage and delay effectiveness–to reflect the test effectiveness of the pattern set. The test coverage of TD (transition-delay) faults is the percentage of the total testable delay faults that ATPG detects: Test coverage=DT/(all faults−UD−AU), where DT is the number of detected faults and UD and AU are the undetectable and ATPG-untestable faults, respectively, that you subtract from the total number of faults. These faults include those in the special SDD-ATPG subcategory of TP (transition partially detected), in addition to DS (detected by simulation) faults detected along their longest paths or paths with slacks satisfying the extended criterion for detection.

Narrowing the scope of SDD ATPG by using the maximum-timing-margin parameter to specify a relatively small maximum timing margin doesn't affect the delay fault test coverage in the equation because the total number of TP faults tends to increase by the same amount as the decrease in DS faults. All other factors being equal, a standard TD-ATPG run and an SDD-ATPG run should produce the same test coverage.

The second SDD-ATPG coverage metric, delay effectiveness, reflects how successful the patterns are in detecting faults through their longest paths. The blue curve plots total fault slack as a cumulative distribution up to 0.5 nsec (Figure A). For each discrete value of slack, a certain number of faults in the design have minimum slacks less than or equal to this slack. For example, about 200,000 faults have minimum slack less than or equal to 0.5 nsec.

The red curve represents the cumulative distribution of detected faults assuming the maximum timing margin for minimum slacks is 0.5 nsec. The faults are distributed according to slacks of their detection paths. For example, of 200,000 faults with minimum slacks of 0.5 nsec or less, ATPG detects about 155,000 faults along paths that have slack that is less than or equal to 0.5 nsec, or 77% of the total.

The detected faults include both DS and TP faults; for both types, the distribution includes only faults that are detected along paths having slacks less than or equal to the maximum-timing-margin parameter. Unless SDD ATPG is successful in detecting every fault along its minimum-slack path, the cumulative distribution of detected faults always stretches right with respect to the cumulative distribution of total faults.

It is possible to calculate the F_D:F_T ratio at any other slack in the domain to determine the effectiveness of the pattern set. For instance, at a slack of 0.2 nsec, the ratio is 72%. Instead of having as many ratios for delay effectiveness as the number of slack intervals, a single metric accounts for the entire range of slacks. Delay effectiveness is typically defined as the ratio of the integrals: Delay effectiveness=$\int F_D(t)dt/\int F_T(t)dt$.

Delay effectiveness is equivalent to the area under the red curve divided by the area under the blue curve–approximately 75% in this example. Narrowing the scope of SDD ATPG by decreasing the maximum timing margin may compromise the delay effectiveness depending on the shape of the cumulative distribution of detected faults in the slack domain. Increasing maximum delta, however, decreases the number of delay faults detected at their minimum slack, stretching $F_D(t)$ to the right and reducing delay effectiveness.

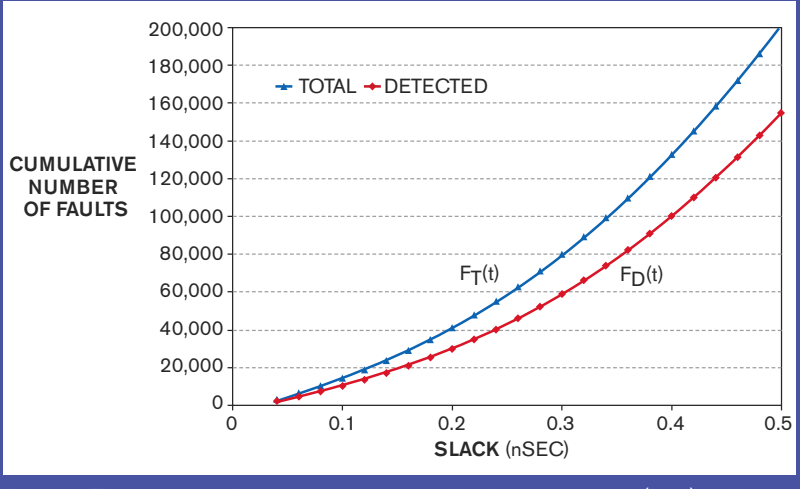


Figure A These curves show cumulative slack distributions of total (blue) and detected (red) transition-delay faults up to 0.5 nsec.

lar to these for other designs; SDD tests consistently screen more failures than any other type of production test in use at STMicroelectronics, reducing DPPM levels relative to rates achievable using standard TD tests.

SMALL-DELAY PREDICTIONS

Recent advances in design-automation technologies have enabled semiconductor companies to efficiently target SDDs during manufacturing test. This development has ensured that, despite Moore's Law, very high defect coverage will be achievable on a consistent basis in the years ahead. Designers will increasingly adopt SDD testing as the primary means of maintaining low DPPM levels as they take advantage of ever-smaller geometries to squeeze more functions onto chips. EDN

REFERENCES

1. Nigh, P, and A Gattiker, "Test method evaluation experiments and data," *Proceedings of the International Test Conference*, pg 454, IEEE 2000, http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=894237.
2. Park, ES, MR Mercer, and TW Williams, "Statistical delay fault coverage and defect level for delay faults," *Proceedings of the International Test Conference, 1988*, pg 492, IEEE, http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=207761.
3. Braun, Alexander E, "Pattern-Related Defects Become Subtler, Deadlier," *Semiconductor International*, June 1, 2005, www.semiconductor.net/article/196943-Pattern_Related_Defects_Become_Subtler_Deadlier.php.
4. TetraMax ATPG User Guide, Version B-2008.09, Synopsys, www.synopsys.com.

AUTHORS' BIOGRAPHIES

Roberto Mattiuzzo is manager of the digital-test-solutions group at STMicroelectronics' technology-R&D organization, where he drives the development and direction of structural test and its deployment to internal business units. You can reach him at roberto.mattiuzzo@st.com.

Davide Appello manages DFX technologies in the system-to-silicon unit of the automotive group at STMicroelectronics, where he implements test, diagnosis, quality, reliability, and DFM methodologies. You can reach him at davide.appello@st.com.

Chris Allsup is marketing manager in Synopsys' synthesis-and-test-marketing group. He has more than 20 years' combined experience in IC design, field applications, sales, and marketing. You can reach him at allsup@synopsys.com.

A version of this article appeared in the June 2009 issue of *Test & Measurement World*.

Go to www.edn.com/090709df2 and click on Feedback Loop to post a comment on this article.

For more technical articles, go to www.edn.com/features.

BY RICK NELSON • EDITOR-IN-CHIEF

EDA COMPANIES TOUT RF DESIGN, LINKS TO TEST

FROM RF/MICROWAVE-CIRCUIT-DESIGN TOOLS TO ELECTROMAGNETIC SIMULATION, EDA COMPANIES WORK WITH INSTRUMENT VENDORS TO GET HIGH-PERFORMANCE, HIGH-QUALITY PRODUCTS TO MARKET.

AWR's Microwave Office comes with Anritsu's new VectorStar Broadband ME7828A system, which operates over the 70-kHz to 110-GHz frequency range (courtesy Anritsu).

EDA companies are introducing tools targeting RF/microwave design and simulation, often working to ensure that their software tools play well with instruments. Test-equipment makers in turn frequently cooperate with EDA providers to ensure that engineers will be able to design and characterize these new devices and systems. The efforts of these diverse companies came into focus at the IMS (International Microwave Symposium), which took place June 7 to 12 in Boston.

On the design side, IMS newcomer Synopsys Inc was on hand to preview its Galaxy Custom Designer 2009.06 release, which it introduced last month. The 2009.06 release adds new capabilities, including high-capacity, high-performance schematic-driven layout designed for large analog blocks. Ed Lechner, director of product marketing for custom design at Synopsys, says that the product builds on the Custom Designer version the company released last September to increase productivity for custom designs in an open environment as process geometries shrink to 45 nm and below.

Custom Designer offers time-saving analysis setup, run, save, and recall features; it provides hierarchical mixed text and schematic representations; and it supports cross-probe and schematic annotation with simulation results. It forms the basis of a complete implementation, physical-verification, circuit-simulation, and analysis flow, integrating with HSpice, CustomExplorer, Cadabra, IC Validator, Star-RCXT, and CustomSim.

The product works with other Synopsys tools for analysis, modeling, and extraction (**Figure 1**). Lechner describes an RF flow using Custom Designer for schematic capture, HSpice RF for circuit simulation, Custom WaveView for analysis, Custom Designer for layout, IC Validator for design-rule checking, Star-RCXT for parasitic extraction, and CustomSim for verification. (For more on this product, see "Tool targets increased productivity in analog environment," *EDN*, this issue, pg 10).

In addition, Synopsys offers TCAD (technology-computer-aided design) for device modeling, as well as DesignWare IP (intellectual property), which includes blocks for complete FSK (frequency-shift-keying) radios, GPS (global-positioning-system) transceivers, mobile-TV tuners, and UWB (ultra-wideband) transceivers. The company also offers the Sentaurus device-simulation tool for multidimensional analysis and the Raphael interconnect-field solver.

FLEXIBLE SIMULATION CHOICES

Also exhibiting at the IMS, CST (Computer Simulation Technology) announced several new capabilities. First, the company now offers flexible simulation acceleration options such as multi-CPU processing, GPU (graphics-processing-unit) processing, cluster computing, and distributed computing. To protect customer investments and to facilitate the choice of the most effective acceleration approach for a given simulation model, CST has introduced a token pricing scheme that enables access to various simulation-acceleration options.

The company also presented a new CST Microwave Studio solver module for electrically large structures; the module supports engineers working on applications such as antenna

placement and radar cross-section simulation. The new module targets a range of simulation-model sizes beyond 100 wavelengths.

"Our customers appreciate our work exploring new regimes in electrical size," says Bernhard Wagner, PhD, managing director of sales and marketing at CST. "The introduction of our integral-equation solver in 2006 fulfilled the needs of one customer segment, but we have noticed a strong tendency toward simulating even larger structures within our design environment." CST is responding to this demand with the introduction of the asymptotic solver, which will be available in CST Studio Suite 2010, due for release in January 2010. CST also announced that the CST Microwave Studio frequency-domain solver will feature third-order and mixed elements with the 2010 release. Version 2010 will feature third-order elements alongside the already-available first- and second-order elements.

ADDING LINKS

Illustrating design companies' efforts to work with test vendors, EDA-software provider AWR at IMS 2009 introduced AWR Connected for R&S (Rohde & Schwarz), which integrates the capabilities of R&S WinIQSIM2 simulation software within AWR's VSS (Visual System Simulator) system-analysis software. The integration of R&S WinIQSIM2 gives VSS access to the range of digitally modulated signals, including those for 3GPP (Third Generation Partnership Project) LTE (long-term evolution), 3GPP FDD (frequency-division duplex)/HSPA (high-speed packet access)/HSPA+, and WiMax (worldwide interoperability for microwave access), which R&S WinIQSIM2 generates, thereby ensuring that engineers simulate their designs with the same signal as a device will encounter in service.

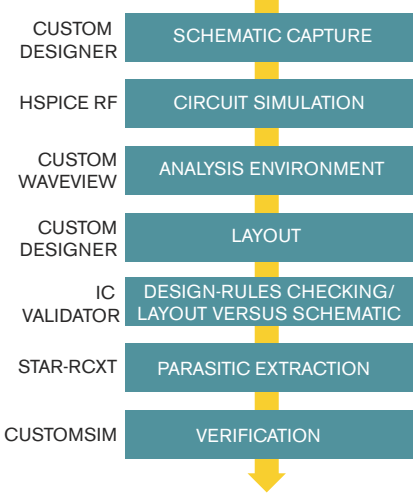


Figure 1 Galaxy Custom Designer works with other Synopsys tools to implement a complete RF-design flow that includes analysis, modeling, and extraction.

AT A GLANCE

- The recent IMS (International Microwave Symposium) highlighted the efforts of diverse companies to collaborate to ensure that their products can communicate.
- Computer Simulation Technology's Microwave Studio solver module targets a range of simulation-model sizes beyond 100 wavelengths.
- AWR introduced products that work with instruments from both Rohde & Schwarz and Anritsu.
- Agilent is focusing on synchronization of LXI (LAN extensions for instrumentation) and new paradigms in data visualization and analysis.
- Tektronix and Mesuro teamed up to demonstrate open-loop, active-harmonic, load-pull-system measurements.

For cross-domain simulations, you can integrate hardware components into any simulation. The signals that an R&S instrument generates return to VSS so that designers can optimize the device under test in VSS to meet the performance goals of wireless-network standards. The cross-domain simulation works with R&S vector-signal generators, such as the SMU200A, which offers RF and baseband capabilities and supports MIMO (multiple-input/multiple-output) measurements.

The R&S liaison isn't AWR's first collaboration with an instrument maker. In January, AWR announced AWR Connected for Anritsu, which makes AWR's Microwave Office high-frequency-design software a standard component of Anritsu's VectorStar MS4640A vector-network analyzer. The VectorStar MS4640A system physically integrates a suite of design tools within its firmware. Microwave Office also comes with Anritsu's new VectorStar Broadband ME7828A system, which operates over the 70-kHz to 110-GHz frequency range. "Integration of Microwave Office software as a standard feature in the VectorStar MS4640A complements this unique instrument's performance and brings an innovative paradigm to the world of microwave simulation and measurement," says Sherry Hess, vice president of marketing at AWR.

Instruments and design tools have for some time been communicating with each other. In 2003, for example, AWR announced that its TestWave software would link Microwave Office and VSS with instruments having RS-232, IEEE-488, or LAN interfaces (**Reference 1**). About the same time, Agilent Technologies introduced its Connected Solutions platform, which allows the sharing of algorithms and data between Agilent instruments and its ADS (Advanced Design System) EDA tool.

NONLINEAR BEHAVIOR

At this year's IMS, Agilent highlighted the ability of its instruments and its EDA software to tackle the modeling,

Figure 2 Darlene JS Solomon of Agilent Labs says that efficiency requirements are driving designers to operate active components in nonlinear regions, making S-parameter measurements insufficient for adequately characterizing devices (courtesy Agilent Technologies).

Figure 3 In conjunction with Maury Microwave, Agilent at IMS 2009 demonstrated the measurement and simulation of nonlinear component behavior, using an Agilent PNA-X nonlinear-vector-network analyzer and Maury Microwave tuners and software (courtesy Agilent Technologies).

Figure 4 Tektronix teamed up with Mesuro at IMS 2009 to demonstrate open-loop, active-harmonic, load-pull-system measurements using the Tektronix arbitrary-waveform generator and sampling oscilloscope plus the Mesuro MB 20 system.

design, simulation, and test of components exhibiting nonlinear behavior. According to Darlene JS Solomon, chief technology officer and vice president of Agilent Labs, efficiency requirements are driving designers to operate active components in nonlinear regions (**Figure 2**). These requirements make S-parameter measurements, which have been the fundamental microwave-measurement approach over the past 40 years, insufficient for adequately characterizing devices. Further, says Solomon, parameters such as the TOI (third-order intercept) and the 1-dB compression point only roughly describe nonlinear behavior. She calls X parameters, a superset of S parameters, a breakthrough approach for measuring large and small signals and outlines how Agilent's nonlinear vector-network analyzers and EDA software support X-parameter techniques.

Solomon notes that Agilent has been serving the RF/microwave industry for more than 60 years, having introduced a signal generator in 1943. In addition to X parameters and nonlinear measurements, two other areas of interest at Agilent are synchronization of LXI (LAN extensions for instrumentation) and new paradigms in data visualization and analysis.

"Increasingly, complex measurement and control problems require coordinated, integrated data acquisition and signal generation," she says. Designers can accomplish these tasks using the time-synchronization features in the LXI standard. Solomon cites LXI applications ranging from flight-test instrumentation to cellular-backhaul measurements. Regarding data visualization and analysis, she says, "Until recently, test-and-measurement systems have focused on getting the best data. Now, [customers] must be able to effectively use complex data sets to make decisions as quickly as possible."

On the show floor, Agilent was one of many companies exhibiting test equipment (**Reference 2**). Among the demonstrations at Agilent's booth was, in conjunction with Maury Microwave, a nonlinear arbitrary-load X-parameter-measurement capability (**Figure 3**).

Tektronix and Mesuro were also focusing on nonlinear measurements. The two companies teamed up to demonstrate open-loop, active-harmonic, load-pull-system measurements using the Tektronix AWG7122B arbitrary-waveform generator and DSA8200 sampling oscilloscope plus the Mesuro MB 20 system (**Figure 4**).

In related news, IMS exhibitor Cadence Design Systems Inc announced the week after the show that Kaben Wireless Silicon had achieved performance boosts while running top-level simulations using the Cadence Virtuoso Accelerated Parallel Simulator (**Reference 3**). Kaben, a provider of RFIC semiconductor IP for wireless communication, credited the Virtuoso Accelerated Parallel Simulator with enabling engineers to find and resolve design issues that they believe they would have otherwise missed. EDN

FOR MORE INFORMATION

Agilent Technologies
www.agilent.com

Anritsu
www.anritsu.com

AWR
www.awrcorp.com

Cadence Design Systems
www.cadence.com

Computer Simulation Technology
www.cst.com

Kaben Wireless Silicon
www.kabenwireless.com

Maury Microwave
www.maurymw.com

Mesuro
www.mesuro.com

Rohde & Schwarz
www.rohde-schwarz.com

Synopsys
www.synopsys.com

Tektronix
www.tek.com

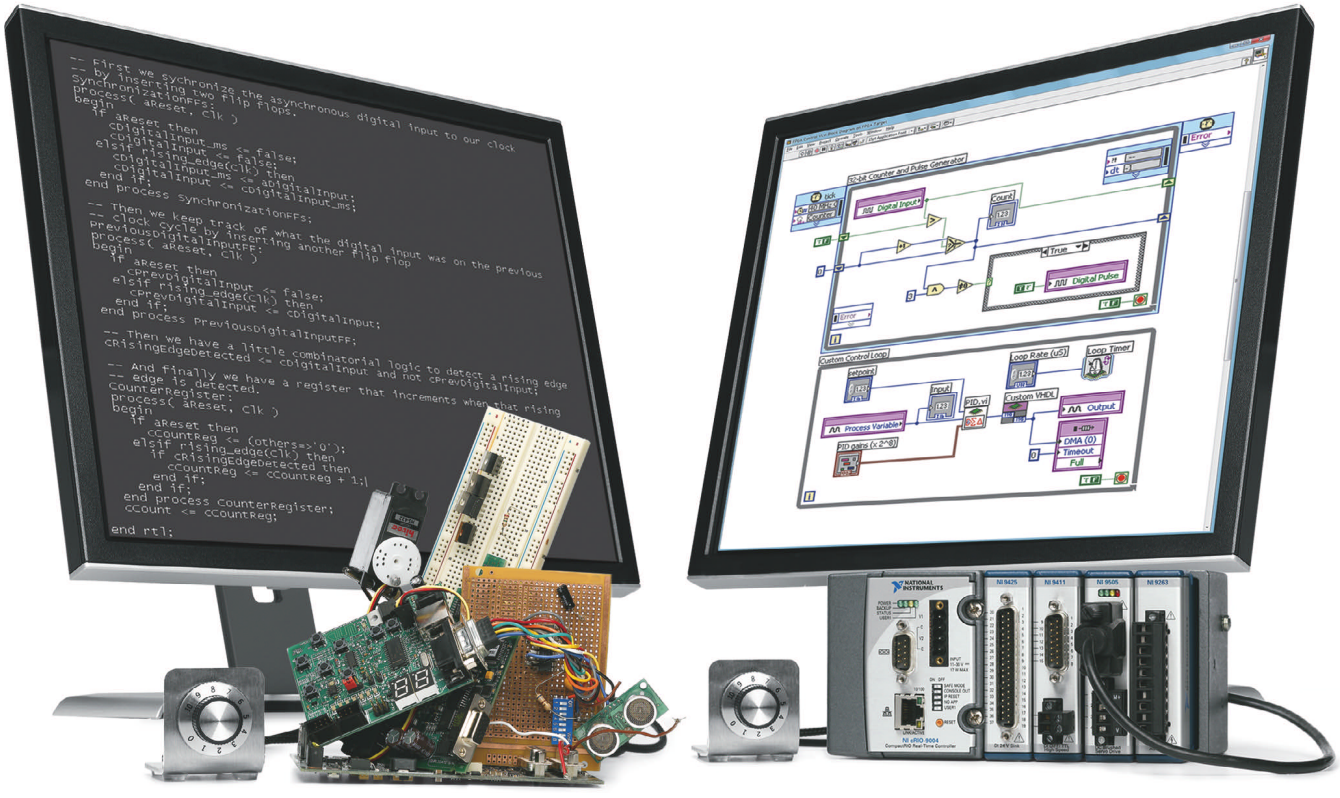
REFERENCES

1 "Test integrates with design at wireless conference," *Test & Measurement World*, April 2003, pg 12, www.tmworld.com/article/CA287086.

2 "From microwave microscopy to 110-GHz analysis," *Test & Measurement World*, July 2009, pg 13, www.tmworld.com/2009_07.

3 Nelson, Rick, "Cadence unveils parallel circuit simulator for the verification of complex analog- and mixed-signal IC designs," *EDN*, Dec 12, 2008, www.edn.com/article/CA6622070.

Embedded Prototyping. Simplified.



Traditional Prototyping Tools **Graphical System Design Tools**

Get to market faster and reduce development costs with graphical system design, an approach that combines open, graphical software and off-the-shelf hardware to help you quickly iterate on designs and easily implement them on an NI embedded platform. The NI CompactRIO system offers an ideal embedded prototyping platform with a built-in microcontroller, RTOS, programmable FPGA, integrated signal conditioning, and modular I/O, as well as tight integration with intuitive NI LabVIEW software.

>> Learn how to simplify embedded design at **ni.com/embedded** **888 279 9833**

NATIONAL INSTRUMENTS™

BY BRETT MURPHY AND AMORY WAKEFIELD • THE MATHWORKS

Early verification and validation using model-based design

WITH A MODEL-CENTRIC APPROACH, EMBEDDED-SYSTEM DESIGNERS CAN VERIFY AND VALIDATE THEIR PRODUCTS AS A PARALLEL ACTIVITY THROUGHOUT THE DEVELOPMENT PROCESS.

When The MathWorks introduced Matlab technical-computing software more than 20 years ago, many of the first users were control-system designers. Anyone who had laboriously inverted matrices by hand to crank through to a controller design fell in love with Matlab at first sight.

Matlab simplified linear-control design, but, in the real world, systems are seldom linear. So even after you designed the controller, testing and tuning it meant building a hardware prototype of the system and coding the algorithm. In other cases, there was no prototype, so testing couldn't take place until late in the development process.

To help verify algorithms before committing them to hardware, engineers turned to numerical techniques to simulate the behavior of the system that the algorithm would control, or the "plant." Control engineers learned to hack C or Fortran programs together to try to model the system, borrowed numerical integration routines that they thought might work for their type of system, duplicated their control algorithm in the system-model program, and simulated the whole thing. This entire simulation-development process was time-consuming and challenging—if you could make it work at all.

The MathWorks in 1990 released Simulink, a software environment for modeling and simulating dynamical systems. Using Simulink in control design offered two big advantages. First, it provided an intuitive, block-diagram environment for modeling both the algorithms and the plant, as well as nonlinear, real-world effects that might affect system behavior. Second, it included a simulation engine that its creators based on state-of-the-art numerical-integration methods. These core features greatly simplified control engineers' task of verifying controllers through simulation. But control engineers still had to eventually code algorithms to test them on hardware prototypes or actual systems.

This process got much easier about five years later with the introduction of automatic code generation from Simulink models. Control engineers no longer had to worry about errors from translating the algorithm model into code for debugging and testing the code running in the prototype system.

The next step in the evolution of control engineering was a major challenge: production-code generation. Rapid prototyping code generally contains a lot of debugging routines, data-collection code, host-target communications code, and other additions useful for interactive testing. Generally, this code was not streamlined enough for deployment in the deliverable system. Code-generation tools evolved to produce code efficient enough to deploy in the production embedded system. Today, many industries consider automatic code generation from control models for production deployment a best practice.

MODEL-BASED DESIGN

The rapid growth in processor speed and memory that enabled the development of modeling, simulation, and code-generation tools on the desktop also enabled embedded-software developers to increase the functions and complexity of embedded controllers. This step in turn drove the need to move beyond traditional code-development techniques using text editors and debuggers to center design on models. This model-centric development approach is known as model-based design (**Figure 1**).

With model-based design, teams use models to develop their

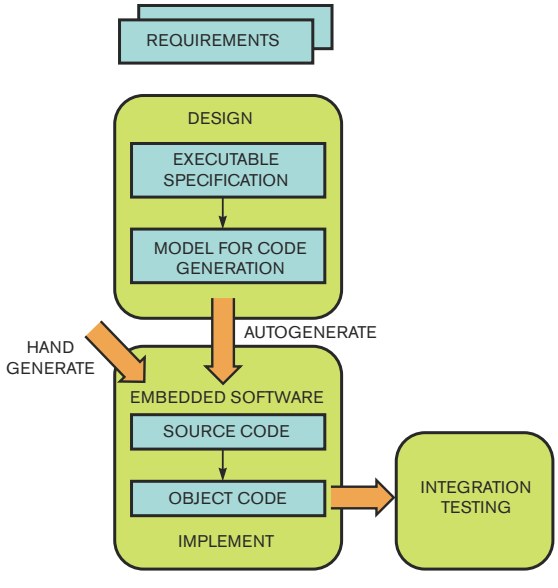


Figure 1 Model-based design streamlines embedded control design with modeling, simulation, and automatic code generation.

designs from the written requirements. With a simulation engine, these models become an "executable specification." The ability to execute the design is a huge benefit to a team trying to develop and review a specification. Once you have reviewed the high-level model, you embellish the model with design details in preparation for translating it into code. Automatic code generation from the detailed design models greatly streamlines the implementation process and removes the chance of introducing translation errors going from the design to the code.

Embedded control systems have traditionally followed the V diagram as a development process (**Figure 2**). This process leaves all verification and test on the right side of the V, after design and implementation are complete. For a traditional, C-code-based embedded-control-development process, integration testing often precedes other forms of increasingly high-level testing, such as hardware-in-the-loop testing and final system test with the actual system under control. Although this development sequence has helped organize complex system design, it does have some drawbacks: The sequence does not consider verification and test until the end, when it is most expensive and time-consuming to fix any errors you find; you must implement all components to test a system; and it fails to account for iteration in a development process.

Model-based design enables the use of verification as a parallel activity that occurs throughout the development process (**Figure 3**). Doing test and verification along every step of the development process means finding errors at their point of introduction. You can reiterate, fix, and verify the design faster than in the traditional V-diagram process. How do you go about achieving early verification, therefore lessening the time you spend at the end of development testing and debugging your design? The following sections outline some best practices.

MODEL VERIFICATION AND VALIDATION

The primary way model-based design achieves verification and validation is through testing in simulation. Although

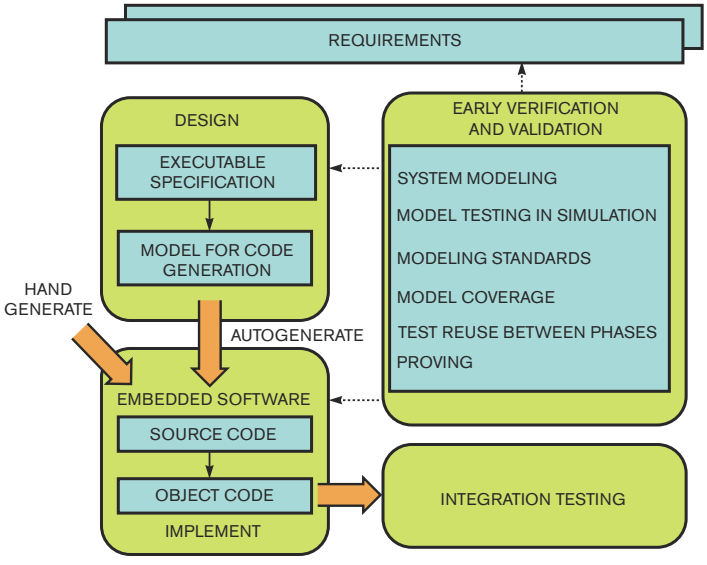


Figure 3 Model-based design enables new techniques for verification and validation to help teams find and fix errors early in requirements, designs, and code.

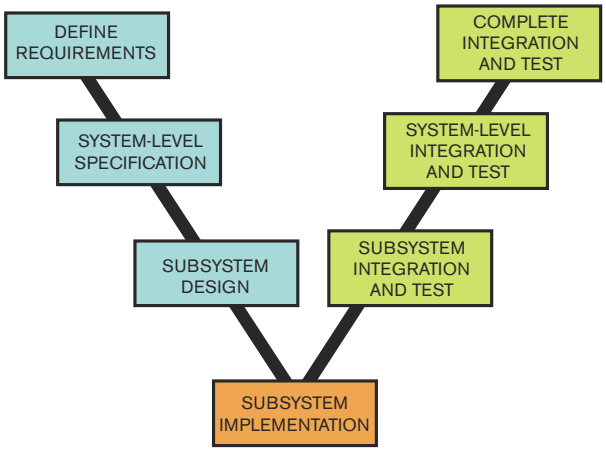


Figure 2 You can capture the traditional embedded-system process as a V diagram showing the reliance on test and verification on the right side of the V, late in the development process.

many organizations do some form of modeling, too many apply simulation in an ad-hoc manner that does not maximize the potential verification benefits. Simulation alone cannot find all errors; however, it is a huge step forward, and you can do it almost as soon as you design a model. Iterating in a modeling environment is fast and easy.

Modeling individual components is useful and may be necessary to complete a complex design; however, don't let that advantage stop you from first modeling the system or environment your component will operate in. By modeling the whole system in a single environment, you can quickly see how the functions of your component will interact with other components and how the integrated components will behave in the deployed system or environment. You can find missing requirements for your component or others. By having a system model to return to as you iterate one component, you can assess how design iterations will affect system functions.

Developing tests in parallel to design and development allows early detection of potential problems, and it significantly reduces the cost and time required for fixing them. By thinking about testing while you develop the model, you will design better for testability, thus ensuring that the design is fully testable. This principle applies far outside the embedded-system area, but embedded-system developers often overlook it. Maybe it is a case of thinking that you can do anything in software, or maybe the documented development process overlooks it. As with new agile-software-development processes, however, developing tests before or in parallel with the design models is a best practice.

Almost every testing scenario involves varying something: inputs, plant parameters, environmental factors, or other elements. Time and expense often limit how much variability you can test for; however, by testing in a simulation environment, you can simulate test cases more quickly and, if the processing power is available, in parallel. Exploring the entire parameter space in simulation can also narrow down the critical tests to run in real time.

Every organization has standards or best practices for design and implementation. Many of these standards are undocumented but exist in key people's heads. Formalizing the standards and incorporating standard checks into your model-development

process is straightforward but can have a large impact by reducing early the number of "silly" errors, ensuring models are more readable for sharing between team members and are more maintainable in the future. Modeling standards can be as simple as verifying that all your inputs and outputs are connected to something as complex as meeting industry standards. The key is developing consistent checks and then driving compliance with them throughout the organization.

Go to www.edn.com/ms4318 and click on Feedback Loop to post a comment on this article.

Determining when a test suite is sufficient is often more art than science because you typically base this determination on the judgment of a design or test engineer. For software components, many teams use code coverage as a more objective measure of test completeness. You can similarly use model coverage for model testing. Coverage is a measure of how much of the logic in a model—or in source code—you exercise during testing. Modified condition/decision coverage is a stringent, well-accepted measure of coverage.

A core principle of most quality standards is to document. Document your requirements. Document your process. Document your results. Without documentation, it is impossible to trace what you did; it is impossible to show someone, such as a customer, that you met his needs; and it is impossible to repeat your results. Although documentation is often tedious, many tools help automate documentation activities by generating standard reports. It is also impossible to overestimate the time savings good documentation will provide if you discover a problem later or you want to reuse a design.

CODE VERIFICATION

These practices are a great starting point for early verification at the model level. Eventually, implementation and deployment onto production hardware become necessary. At this point, code verification becomes the focus. How does model-based design help?

Automatic code generation is one method that helps. By verifying your design at the model level and then generating code directly from it, you need verify only that the model and code are equivalent. This workflow is ideal. In the real world, it is sometimes impossible to generate all the code you need from a model. You may have middleware and device-driver code that you develop using traditional processes, or you may use legacy code for some functions. For these cases, there are some additional best practices to verify code.

You can test hardware almost everywhere; however, it is often disconnected from testing in simulation. Many factors can drive that disconnection: Groups who run tests on hardware differ from those who model the design, and the software that runs in the lab differs from the software in the design. However, when you run the same tests on your model that you run in the lab, you know exactly how the design should perform in the lab. To verify the equivalence of code to the design model, you can use the same test harness for model testing to test the software implementation of the model compiled and running on the embedded target. Running tests on a component design model simultaneously with code on an embedded target is a co-simulation step called PIL (processor-in-the-loop) testing. Tools are now available to execute the tests—which a developer created on a host computer, such as a PC—on the software synchronously with running it on an embedded processor. Comparing test results of the embedded code with the original model helps you ensure that the behavior of the component remains unchanged after compilation and downloading and that the code is functionally correct.

Runtime errors in embedded code can be especially challenging to find, and, once you find them, they are difficult to debug. Examples include overflows and underflows, division by zero and other arithmetic errors, out-of-bound array access, illegally dereferenced pointers, read-only access to noninitialized data, and dangerous type conversions. Until recently, there were essentially only three options for detecting runtime errors in embedded software: code reviews, static analyzers, and trial-and-error dynamic testing. Code reviews are labor-intensive and often impractical for large, complex applications. Static analyzers identify relatively few problems and, more important, fail to diagnose most of the source code. Dynamic, or "white-box," testing requires that you write and execute numerous test cases. When tests fail, debugging the problem can be difficult. Code-verification tools, based on formal methods, allow you to prove the absence of runtime errors and provide strong assurance of the code's reliability. When you use them in addition to testing, as part of a development process, code-verification tools provide other techniques for identifying design and implementation errors that would be difficult to find and costly to correct in later testing phases.

System modeling and simulation tools, such as Simulink, help streamline the task of designing and verifying complex algorithms without expensive hardware. In place of hand-coded, hard-to-maintain simulations, control designers can quickly develop complex algorithms and system models and test their algorithms before committing them to hardware. Years of experience have given rise to approaches that provide automatic code generation to support real-time testing in prototyping systems and later for deployable embedded code. Today, model-based design sees use in a variety of applications, including controls, image processing, audio, communications, and signal processing.

One of the primary benefits of model-based design is the opportunity to do rigorous verification and validation in parallel with all other development steps, especially early in the development process. You can maximize these benefits using a series of best practices that adopters of model-based design have discovered through hard experience. Practices such as developing tests along with models and reusing model tests on code and hardware, among others, can significantly reduce the risk of a development project missing quality or delivery goals due to the discovery of errors late in the process. EDN

AUTHORS' BIOGRAPHIES

Brett Murphy manages the technical-marketing teams for verification and validation, test and measurement, rapid prototyping, and hardware-in-the-loop products at The MathWorks. He holds bachelor's and master's degrees in aerospace engineering from Stanford University (Palo Alto, CA).

Amory Wakefield is a product manager for simulation and test applications at The MathWorks. She has bachelor's and master's degrees in electrical science and engineering from the Massachusetts Institute of Technology (Cambridge).

EDITED BY MARTIN ROWE
AND FRAN GRANVILLE

designideas

READERS SOLVE DESIGN PROBLEMS

Illumination ring provides focused intensities

William Grill, Honeywell Aerospace, Olathe, KS

If you use a camera-based inspection or soldering fixture, you need to see images in a small area. Often, side lighting produces shadows on an image that result in contrasting colors and poor quality. Thus, your monitor views may be difficult to clearly see or interpret. Centering a light ring on the image provides illumination on all sides of the object and may illuminate everything you need to see. In a camera application for controlling a light ring, this implementation not only controls the light, but also enables you to direct the light intensity by maintaining two levels of control. It also lets you maintain and rotate the second-tier levels about the illuminated object.

Based on a seven-LED set, you select three consecutive LEDs; the second-tier settings will define the three LEDs' intensities (**Figure 1**). The remaining displays are maintained at a base-tier-intensity setting. Using four pushbutton switches, the Microchip (www.microchip.com) 16F505 rotates, distributes, and provides PWM (pulse-width-modulation) control of these two power tiers across the seven LEDs. Two of the buttons increase or decrease intensity, or they group or ungroup the tier-intensity settings; the other two buttons rotate the resulting second-tier display clockwise or counterclockwise.

The implementation uses just a few parts, exploiting the controller to provide light level, state maintenance, and PWM control. The application debounces the buttons and indexes the intensity controls. An eighth LED indicates tier-grouped or -ungrouped

DIs Inside

▶To see all of *EDN*'s Design Ideas, visit www.edn.com/designideas.

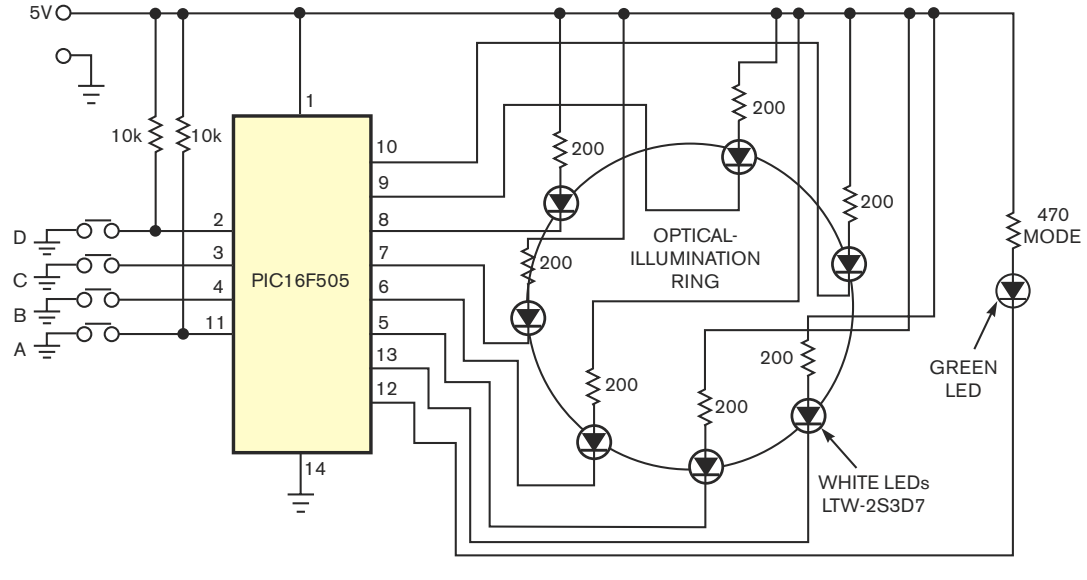


Figure 1 An LED illumination ring provides directed light intensity.

mode. When you group the tiers together, their intensity-setting indexing is common, but their register limits remain independent. You can download **Listing 1**, the assembly code for the circuit, from the online version of this Design Idea at www.edn.com/090709dia.

The controller provides a PWM period of approximately 7.5 msec to all the LEDs. It also controls each LED's duty cycle, according to the registered levels the button sets, in defined and maintained register masks and intensity values. The controller provides six bits of intensity, corresponding to 64 levels of resolution, although 8-bit resolution is available. The operating voltage is 5V. You can reconfigure the controller, the display, and their limiting resistors to operate at voltages as low as approximately 3.1V. High-millicandle, white, 5-mm, T1¾ through-hole LEDs provide the light source. The controller provides about 8 mA of current to each of the LEDs. By constraining the total power, surface-mount or other LED configurations are possible.

You can lay out the four momentary-action pushbutton switches for operation by the left or the right hand. With one representing the pushbuttons' asserted position, the controller's coded sequences provide the button-control functions found in **Table 1**.EDN

TABLE 1 PUSHBUTTON-CONTROL FUNCTIONS

A	B		C	D	
1	1	No function	1	1	Alternate between common-tier mode and second-tier mode
1	0	Select second-tier mode, rotate Tier 2 LEDs counterclockwise	1	0	Increment all or second tier if in second-tier mode with autoindexing
0	1	Select second-tier mode, rotate Tier 2 LEDs clockwise	0	1	Decrement all or second tier if in second-tier mode with autoindexing
0	0	No function	0	0	No function

Digital variable resistor compensates voltage regulator

Jason Andrews, Maxim Integrated Products Inc, Dallas, TX

A variable resistor that integrates a programmable, temperature-indexed look-up table can compensate for the temperature drift of a voltage regulator. In this case, the look-up table can change the resistance every 2°C over a range of −40 to +102°C, thereby nulling any regulator-output changes that would otherwise occur because of temperature. A typical regulator circuit comprises a regulating element, a feedback-resistor divider, and capacitors to provide filtering and regulation against transients and load-switching conditions (**Figure 1**). The ratio of the two feedback-divider resistors sets the regulator-output voltage. The regulator can generate either a preset 3.3V or any user-defined output within its operating range.

For most regulator circuits, the output voltage varies slightly with temperature, from 97.6 to 101.5% of nominal in this circuit. These numbers are respectable, but you can improve them. First, incorporate a digitally controlled variable resistor, such as a DS1859, into the regulator circuit of **Figure 1** by placing it in parallel with R_2 (**Figure 2**). A temperature-indexed look-up table in an internal nonvolatile memory controls the 50-kΩ digital resistor, allowing you to program a different resistance value for each 2°C window.

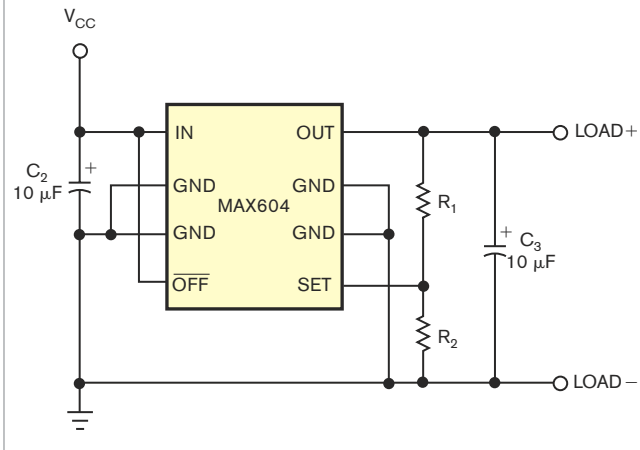


Figure 1 A typical voltage regulator lets you set the regulated output level by adjusting the R_1/R_2 divider.

You can program the look-up table to provide any resistance-versus-temperature profile. In this example, the look-up table flattens the regulator's normal curve over temperature. These look-up tables, therefore, provide a positive resistance slope with respect to temperature. The resistor has 256 programmable resistance settings of 0 to 255 decimal, and each one accounts

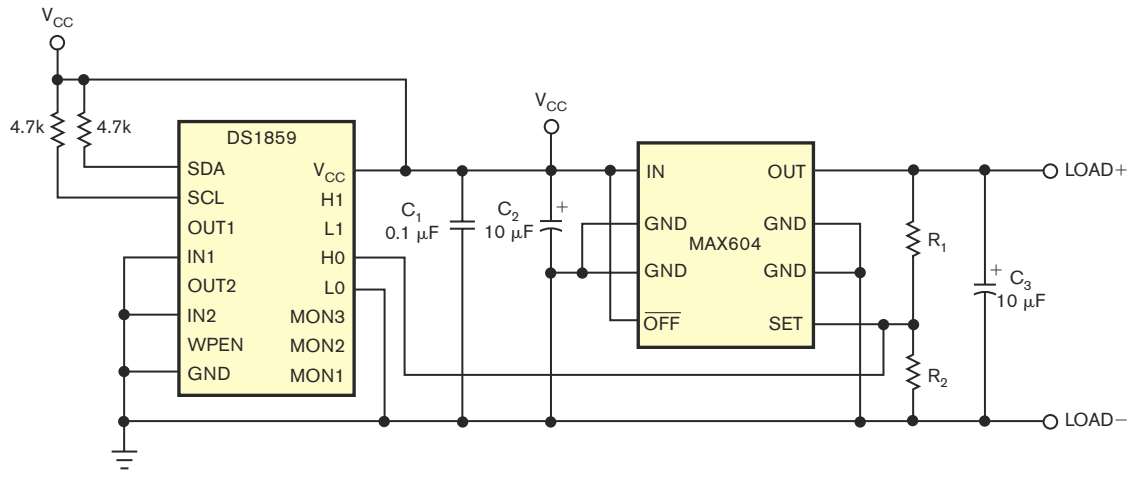


Figure 2 Connecting one-half of a dual variable resistor in parallel with R_2 to the circuit in Figure 1 lets you temperature-compensate the regulated output voltage.

for approximately 192Ω. In this example, the look-up table was programmed with a setting of 143 decimal at −40°C. The settings were incremented by one for every 4 to 6°C change in temperature, resulting in a value of 152 decimal for ambient and 158 decimal for +85°C.

As illustrated in **Figure 3**, the result of this regulated performance over temperature is a drastic increase in precision: The variation from −45 to +85°C is now only ±2 mV. For comparison, note the response of the standard regulator circuit in **Figure 1** (the black curve). The digital-resistor IC of **Figure 2** includes three ADC inputs for monitoring external voltages. An alternative, the DS1847 dual variable resistor, offers similar performance without the ADC monitors and at lower cost. EDN

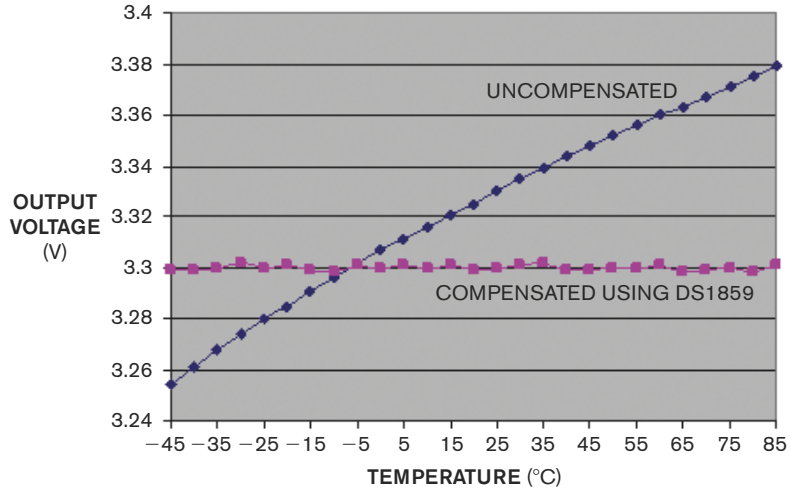


Figure 3 These curves compare regulated outputs versus temperature for the Figure 1 circuit (black) and the compensated Figure 2 circuit (pink).

Hot-swap switch provides easy thermal protection

Donald Schelle, National Semiconductor Corp, Santa Clara, CA

It is often difficult to design an effective thermal-management scheme that minimizes the risk of meltdown or fire. System orientation, placement, or both complicate matters by generating hot spots at varying locations on a PCB (printed-circuit board). A hot-swap switch and carefully placed temperature sensors mitigate thermal issues by disconnecting system power when a temperature exceeds a safe limit. The circuit in **Figure 1** uses a hot-swap switch to monitor overvoltage, undervoltage, and overcurrent conditions. When the ambient temperature exceeds a preset threshold, a carefully placed temperature sensor, IC_1, forces the hot-swap controller, IC_2, to disconnect system power. You can use multiple tempera-

LINEAR TECHNOLOGY

DESIGN NOTES

Maximize the Performance of 16-Bit, 105Msps ADC with Careful IF Signal Chain Design

Design Note 468

Clarence Mayott and Derek Redmayne

Introduction

Modern communication systems require an ADC to receive an analog signal and then convert it into a digital signal that can be processed with an FPGA. The job of a mixed signal engineer is to optimize the signal at the input of the ADC to maximize overall system performance. This usually requires a signal chain comprised of multiple gain and filtering sections. An ADC is only as good as the signal it is measuring.

For instance, the LTC®2274 provides excellent AC performance with an appropriate IF signal chain. The LTC2274 is a 16-bit, 105Msps ADC that serially transmits 8B/10B encoded output data compliant with the JESD204 specification. It uses a single differential transmission line pair to reduce the number of IO lines required to transmit output data. The LTC2274 has 77dB of SNR, and 100dB of spurious free dynamic range.

Signal Chain Topology

Figure 2 details a signal chain optimized for a 70MHz center frequency and a 20MHz bandwidth driving the LTC2274. The final filter and circuitry around the ADC are shown in detail. The earlier stages of the chain can be changed to suit a target application.

The first stage of amplification in the chain uses an AH31 from TriQuint Semiconductor. This GaAs FET amplifier offers a low noise figure and high IP3 point, which minimizes distortion caused by the amplifier stage. It provides 14dB of gain over a wide frequency region. The high IP3 prevents intermodulation distortion between frequencies outside the passband of the surface acoustic wave (SAW) filter.

A SAW filter follows the amplification stage for band selection. The SAW filter offers excellent selectivity and a flat passband if matched correctly. Gain before the SAW must not be higher than the maximum input power rating of the SAW; otherwise it leads to distortion. A digitally controlled step attenuator may be required in the signal path to control the power going into the SAW filter.

The second stage of amplification is used to recover the loss in the SAW filter. The insertion loss of the SAW filter is about –15dB, so the final amplifier should have at least this much gain, plus enough gain to accommodate the final filter. By splitting the gain between two amplifiers, the noise and distortion can be optimized without overdriving the SAW filter. It also allows for a final filter with better suppression of noise from the final amplifier, improving SNR and selectivity.

The output stage of the final filter needs to be absorptive to accommodate the ADC front end. This suppresses glitches reflected back from the direct sampling process.

This signal chain will not degrade the performance of the LTC2274. When receiving a 4-channel WCDMA signal with a 20MHz bandwidth, centered at 70MHz, the ACPR is 71.5dB (see Figure 1).

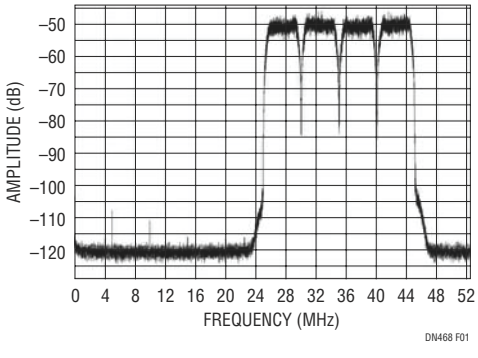


Figure 1. Typical Spread Spectrum Performance

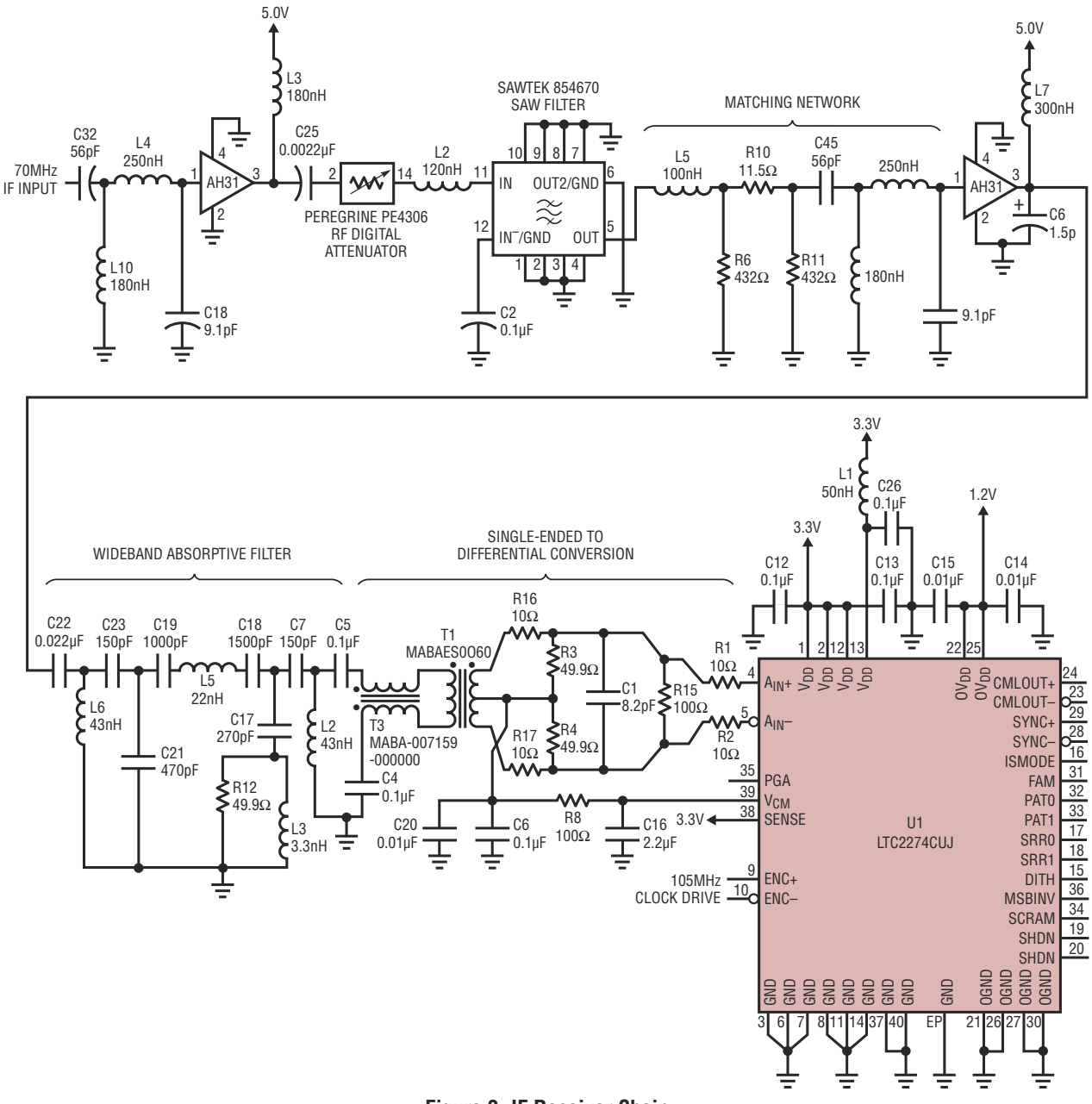


Figure 2. IF Receiver Chain

Conclusion

The LTC2274 can be used to receive high IF frequencies, but getting the most out of this high performance ADC requires a carefully designed analog front end. The performance of the LTC2274 is such that it is possible to dispense with the automatic gain control and build a receiver with a low fixed gain. The LTC2274 is a part of a family of 16-bit converters that range in sample rate from 65Msps to 105Msps. For complete schematics of this receiver network, visit www.linear.com

Data Sheet Download

www.linear.com

For applications help,
call (408) 432-1900, Ext. 2602

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

dn468f LT/TP 0709 116K • PRINTED IN THE USA

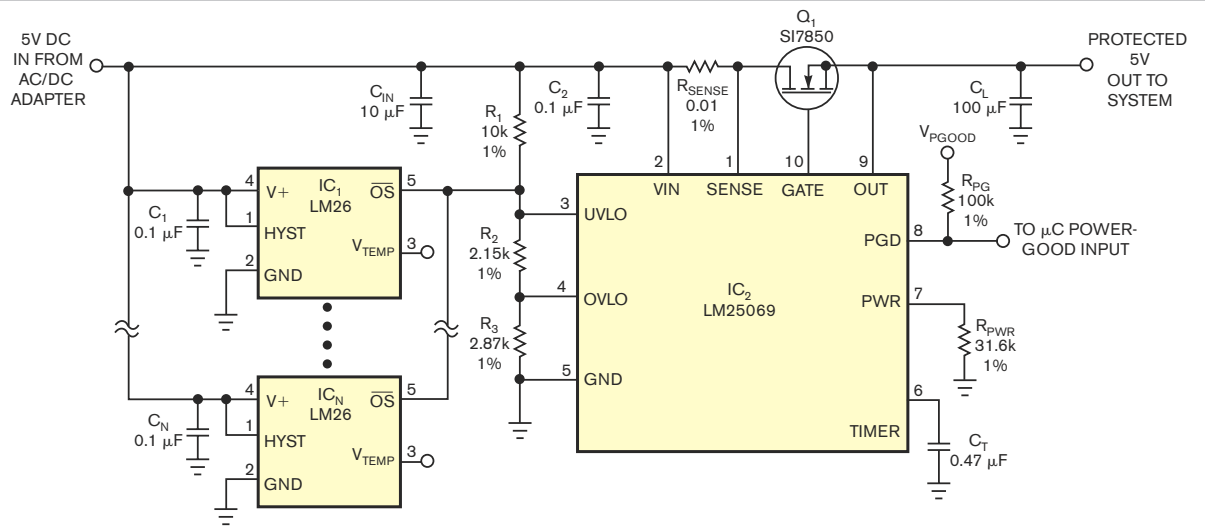


Figure 1 Carefully placed low-cost temperature sensors disconnect system power when an overtemperature thermal event occurs.

ture switches to isolate hot spots when you mount the system in varying orientations. The circuit requires neither a microcontroller nor a costly temperature-monitoring IC. Thermal events cut power to the system using a robust, nondestructive technique.

In a typical overtemperature condition (**Figure 2**), a thermal event (upper trace) causes the LM26 to trip, forcing the LM25069 to disconnect power from the system (middle and lower traces). When the system temperature decreases below the LM26's trip point, system power returns. Incorrect placement or orientation can cause overtemperature events, forcing the system to turn on and off like clockwork; support personnel can easily diagnose this symptom. Inexpensive temperature sensors and an innovative power-limiting hot-swap controller reduce the cost of this circuit to approximately $2 in low-volume applications. EDN

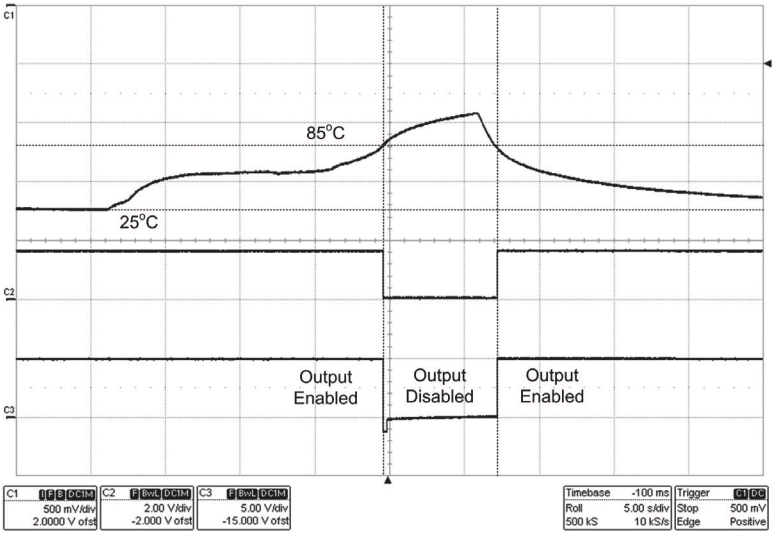


Figure 2 As the temperature rises above the threshold (top trace), the output of the temperature sensor (middle trace) goes low, forcing the hot-swap switch to disconnect power (bottom trace) from the circuit.

Add headphones to a Class D amplifier

Hiroshi Fukushima, Technical Research Center,
D&M Holdings Inc, Kawasaki City, Kanagawa, Japan

The MAX9704 from Maxim (www.maxim-ic.com) is a small and efficient Class D audio power amplifier. Its fully balanced inputs and Class D outputs make it a convenient chip to directly drive speakers. Sometimes, though, you want to have a headphone output to keep the office environment. Class D power amplifiers usually have fully balanced, bridged outputs on each channel. If the amplifier drives separate speakers, you can use an attenuator circuit (**Figure 1**). A problem arises, however, with grounded headphones: Stereo headphones use three-pole plugs with which the negative side of each speaker connects to a common ground. Thus, you may think that you can't directly connect head-

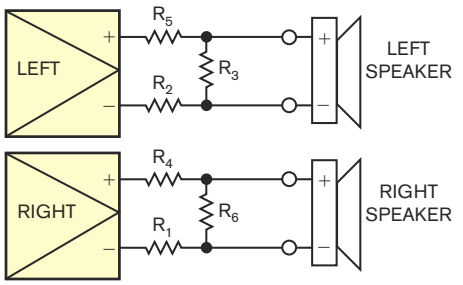


Figure 1 A Class D amplifier has separate drivers for each speaker.

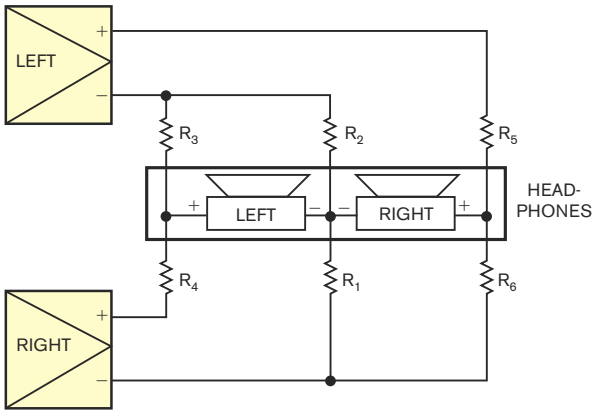


Figure 3 This speaker configuration lets you connect headphones with a common ground to a Class D amplifier.

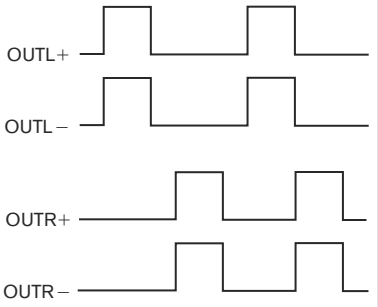


Figure 2 The MAX9704 applies power to one channel at a time.

phones to a Class D amplifier without using a transformer.

To solve the problem, look at the output waveform of the MAX9704 as it swings (**Figure 2**). Each channel output alternates between high and low. You can take advantage of the fact that the channels aren't on at the same time by configuring your circuit like the one in **Figure 3**.

Figure 4 shows the circuit details. Because the MAX9704 alternates the outputs of each channel, the R_3/R_6 combination doesn't affect the channel's drivers. Resistors R_3 and R_2 connect to the left output terminal. Resistors R_4 and R_1 connect to the right output terminal. The inactive channel's output voltage must be the same voltage, which means that R_4, R_1, and R_6 connect to the same voltage when the left-channel output is active. R_3, R_1, and R_5 connect to the same voltage when the right-channel output is active. The values of R_1 and R_2 affect how much crosstalk you get between channels. The values in **Figure 4** provide sufficient channel separation. EDN

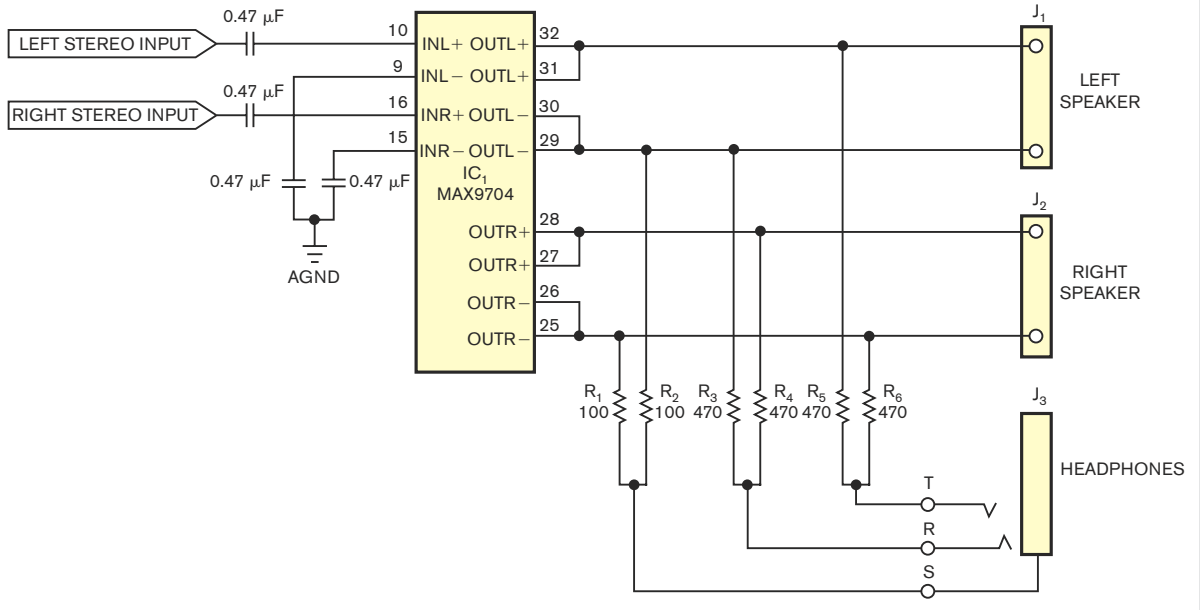
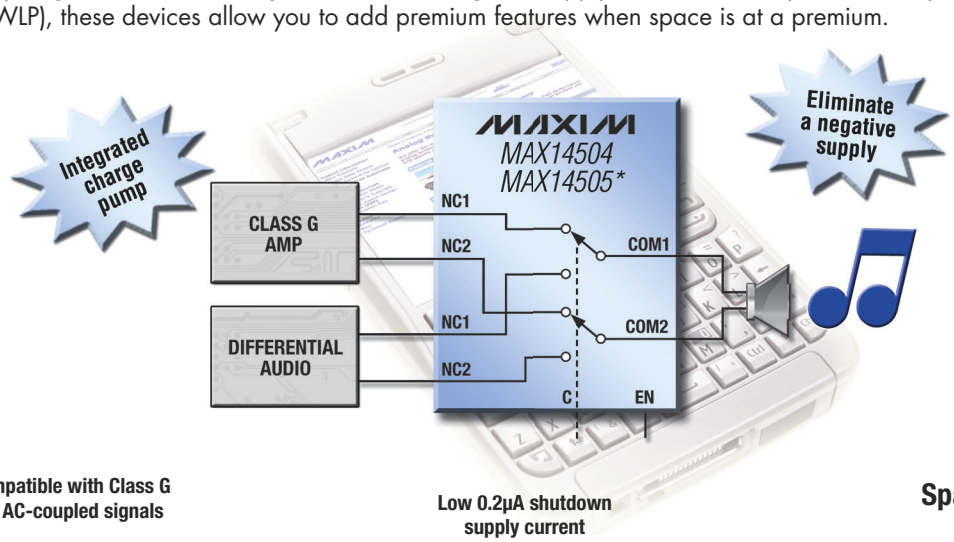


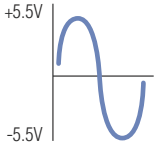
Figure 4 With the resistors in place, you can connect headphones to the MAX9704 amplifier.

Only single-supply switches with ±V_{CC} signal handling

The MAX14504/MAX14505* integrate a charge pump to support the high output-signal range required by Class G and DirectDrive® amplifiers. They thus enable the use of more-compact amplifier topologies while eliminating the need for a negative supply. Offered in a tiny wafer-level package (WLP), these devices allow you to add premium features when space is at a premium.



Compatible with Class G or AC-coupled signals



Low 0.2µA shutdown supply current

Space-saving package

Support high audio quality

- ±5.5V analog signal range
- Low 0.05% THD+N
- Integrated shunt resistors available for click-and-pop suppression

Ideal for portable applications

- 2.5V to 5.5V single-supply operation
- Low 0.2µA shutdown supply current
- Tiny 12-bump WLP

Part	Configuration	Shunt Resistors	Signal Range	Package (mm x mm)
MAX14504	Dual SPDT	—	-V_{CC} to +V_{CC}	12-WLP (1.56 x 2.14)
MAX14505*		NO and NC input		
MAX14505A		NO and NC input	0 to +V_{CC}	
MAX14506*		—		

DirectDrive is a registered trademark of Maxim Integrated Products, Inc.
*Future product—contact factory for availability.

www.maxim-ic.com/MAX14504-info

MAXIM DIRECT™ www.maxim-ic.com/shop

AVNET electronics marketing www.avnet.com

MAXIM INNOVATION DELIVERED™

For free samples or technical support, visit our website.

Circuit eases power-sequence testing

Goh Ban Hok, Infineon Technologies Asia Pacific Ltd, Singapore

Systems on chip (SOCs) normally require one power supply for the core and another for I/O. To properly apply power to the device, you often need one supply to apply power before the other. The circuit in **Figure 1** lets you test the power sequencing of the SOC. Two TPS75501 linear regulators, IC_3 and IC_4, generate two power supplies. The TPS75501 adjustable regulator provides output voltages of 1.22 to 5V from a maximum input of 6V. The circuit uses 5V as the input source, and it can supply as much as 5A. The SOC requires 3.3 and 1.5V. The following **equations** describe how to set the voltages. $V_{OUT1}=V_{REF}\ (1+R_4/R_5)$ for IC_3, and $V_{OUT2}=V_{REF}(1+R_6/R_7)$ for IC_4. The reference voltage is 1.22V.

In the circuit, R_5 and R_7 are 30 kΩ. Variable resistor R_4 is 7 kΩ for the 1.5V supply, and R_6 is 50 kΩ for the 3.3V supply. Green LED D_2 lights when the 3.3V supply is present, and red LED D_1 lights for the input-supply voltage. Pin 1 of the TPS75501 is the enable pin. When low, it enables the output voltage at Pin 4. Switch S_2 selects the sequence of the power supplies. IC_1 is a 555 timer operating as a monostable circuit. It provides the delay between the two power supplies. You can adjust the delay by using the time constant of R_3 and C_3: Delay=$1.1\times R_3C_3$.

C_3 is 33 µF and R_3 is 11 kΩ for a 400-msec delay between powering the two supplies. The timer triggers with a negative pulse at Pin 2 of IC_1. It produces a positive pulse at Pin 3 of IC_1. The output becomes inverted at IC_{2A} before passing to IC_6's Pin 11. IC_5 and IC_6 are the latched circuits. The set pin, S, connects to the 5V supply, and the reset pin, R, connects through resistors R_2 and R_{10} and capacitors C_4 and C_7 to ensure that the Q output is high during the initial power-up stage. Regulators IC_3 and IC_4 are initially off.

When analog switch S_2 is in the on position, the sequence of the 1.5V power supply starts first, and the 3.3V supply follows. To start the power-sequence testing, press and release trigger switch S_1 to momentarily produce

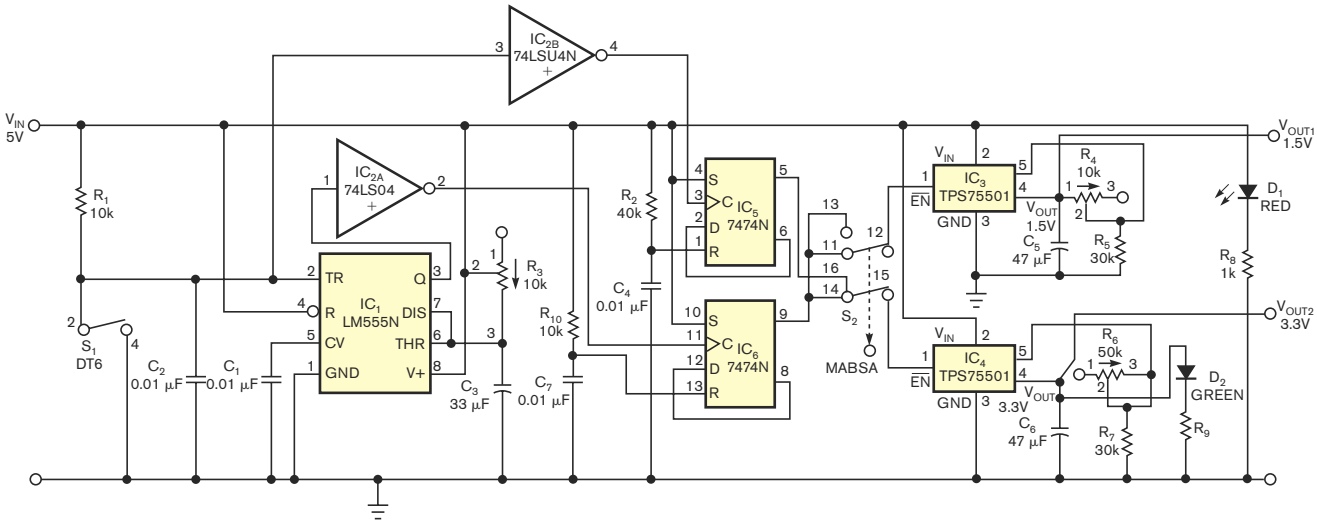


Figure 1 A configurable sequencing circuit uses a 555 timer to delay one power supply.

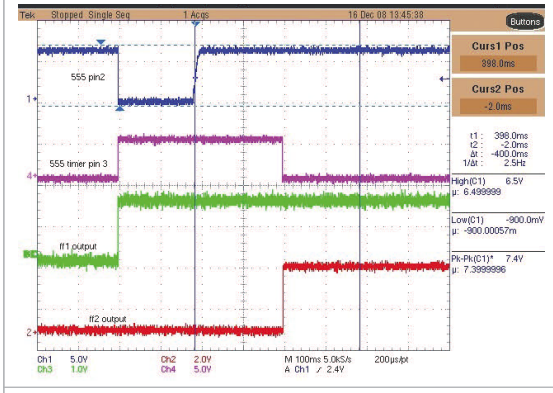


Figure 2 The 1.5V power supply (green trace) comes on first, and the 3.3V supply (red trace) and 555 timer follow.

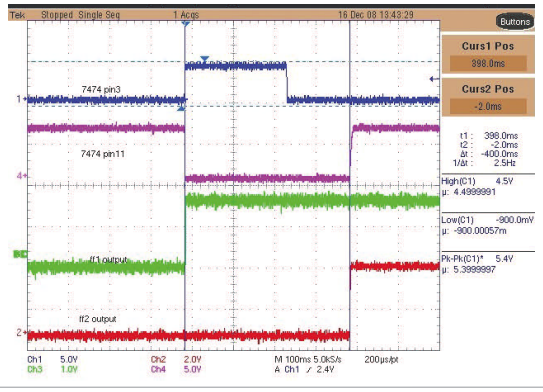


Figure 3 The 1.5V power supply (green trace) comes on first, and the 3.3V supply (red trace) and 7474 latch-circuit input follow.

High-performance, miniature crystal oscillators

Deliver frequencies to 622.08MHz and less than $1ps_{RMS}$ jitter

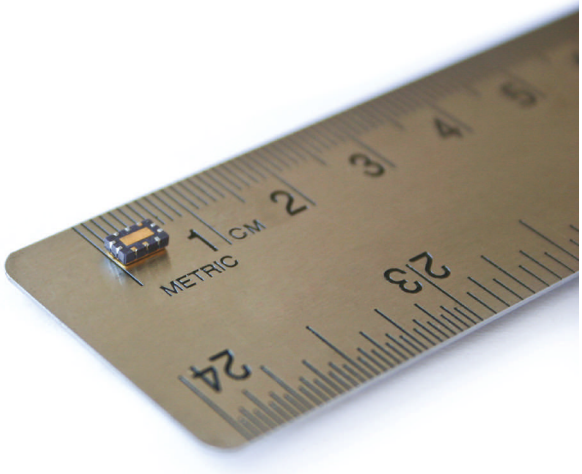
The DS4-XO crystal oscillators use fundamental AT-cut crystals to enhance frequency stability over temperature. They provide higher stability (±50ppm) than SAW-based oscillators (±100ppm) over the extended temperature range, and they eliminate the spurious modes of operation associated with overtone designs. Their miniature ceramic package allows precise placement in designs, thus making them ideal for Fibre Channel, InfiniBand™, and other networking applications.

Features

- **Low jitter: < $1ps_{RMS}$ from 12kHz to 20MHz**
- **Wide frequency range: 77.76MHz to 622.08MHz**
- **Small size: 5mm x 3.2mm x 1.49mm**
- **High frequency stability: ±50ppm (-40°C to +85°C)**
- **Low voltage: 3.3V ±5%**

Applications

- **Fibre Channel:** DS4106, DS4212, DS4425
- **InfiniBand:** DS4125
- **Ethernet, 10GbE:** DS4125, DS4156, DS4312
- **SAS/SATA:** DS4150
- **SONET/SDH:** DS4155, DS4311, DS4622, DS4776
- **PCI Express®:** DS4100H



Housed in a tiny, 5mm x 3.2mm x 1.49mm LCCC ceramic package, the DS4-XO crystal oscillators offer the industry's highest performance and save critical board space.

www.maxim-ic.com/DS4-XO

MAXIM DIRECT
www.maxim-ic.com/shop

AVNET electronics marketing
www.avnet.com

MAXIM INNOVATION DELIVERED™

For free samples or technical support, visit our website.

a low pulse. This pulse triggers the 555 timer, IC_1, which produces a positive pulse. This pulse in turn produces a delay before enabling IC_4's power 3.3V supply. When you press and release S_1, another signal goes to inverter IC_{2B} before passing to the latch pin, Pin 3 of IC_5. There is no delay for the 1.5V regulator that connects to this pin. It enables IC_3's 1.5V power supply. Because IC_3's enable pin immediately receives the enable signal, it produces the 1.5V without delay. IC_4's enable pin, which receives a signal after the delay by the 555 timer, later produces the 3.3V, thus achieving the power sequence. The 1.5V power supply comes first when you press S_1, and the 3.3V power supply comes on only after the 555 timer delay (**figures 2** and **3**).

Switch S_2 connects to pins 13 and 16. When S_2 is off, the power sequence changes. In this case, the 3.3V supply powers up first, and the 1.5V supply follows (**figures 4** and **5**). When you press S_1, the 3.3V power supply comes first, and the 1.5V supply follows after the 555 timer delay. EDN

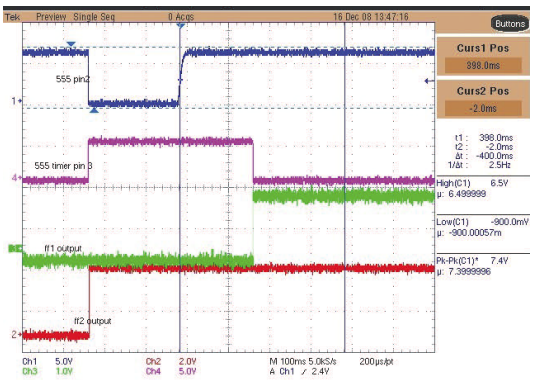


Figure 4 The 3.3V power supply (red trace) comes on first, and the1.5V supply (green trace) and 555 timer follow.

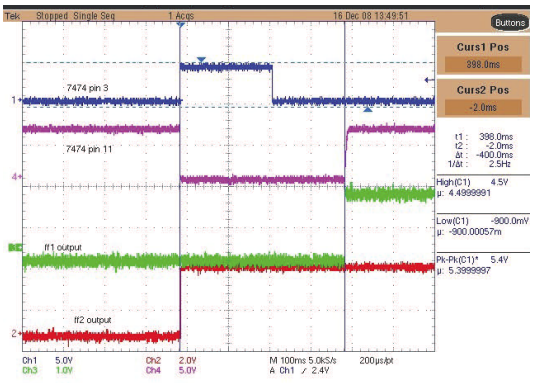


Figure 5 The 3.3V power supply (red trace) comes on first, and the 1.5V supply (green trace) and 7474 latch-circuit input follow.

PICO

SPACE SAVING TECHNOLOGY
Transformers & Inductors from .19" ht.
Over 5000 Standard Surface Mount and Thru-Hole Models

Audio Transformers
Impedance Levels 10 ohms to 250k ohms, Power Levels to 3 Watts, Frequency Response ±3db 20Hz to 250Hz. All units manufactured and tested to MIL-PRF-27. QPL Units available.

Power & EMI Inductors
Ideal for noise, spike and Power Filtering Applications in Power Supplies, DC-DC Converters and Switching Regulators

Multiplex Data Bus Pulse Transformers
Plug-In units meet the requirements of QPL-MIL-PRF 21038/27 Surface units are electrical equivilents of QPL-MIL-PRF 21038/27.

Pulse Transformers
10 Nanoseconds to 100 Microseconds. ET Rating to 150 Volt Microsecond, Manufactured and tested to MIL-PRF-21038.

DC-DC Converter Transformers
Input voltages of 5V, 12V, 24V And 48V. Standard Output Voltages to 300V (Special voltages can be supplied). Can be used as self saturating or linear switching applications. All units manufactured and tested to MIL-PRF-27.

400Hz/800Hz Power Transformers
0.4 Watts to 150 Watts. Secondary Voltages 5V to 300V. Units manufactured to MIL-PRF-27 Grade 5, Class S (Class V, 155°C available).

ISO CERTIFIED 9001:2000

PICO Electronics, Inc.

143 Sparks Ave. Pelham, NY 10803 • ***Call Toll Free*** 800-431-1064 • ***Fax:*** 914-738-8225

Send for free 180 pg PICO Catalog

See PICO's full Catalog Immediately on the internet

www.picoelectronics.com

E-mail: info@picoelectronics.com

Looking to buy?
With BuyerZone, every big deal is no big deal at all.

BuyerZone is the trusted, unbiased site that brings buyers and sellers of business purchases together to make the purchasing process easier while saving both parties time and money. Credit Card Processing, Building Services, Home Security, Trade Show Displays, Forklifts and Construction Equipment, Business Purchases and more... Let us do the work so you don't have to.

Join the millions who've already saved time and money on many of their purchases by taking advantage of BuyerZone's FREE, no obligation services like:

- Quotes from multiple suppliers
- Buyer's guides
- Supplier comparisons
- Pricing articles
- Supplier ratings

REQUEST FREE QUOTES NOW!
Call (866) 623-5525 or visit BuyerZoneQuotes.com

BuyerZone
Where Smart Businesses Buy and Sell

A division of Reed Business Information.

EDITED BY SUZANNE DEFFREE

supplychain

LINKING DESIGN AND RESOURCES

Distributors' education services blossom

Distributor-supplied services extending technical and product education are increasingly in demand as engineering teams at brand owners continue to shrink and the formidable stress on design teams continues to grow. Web-based training is a growing service trend distributors are offering to engineers and suppliers. Newark (www.newark.com), for one, has produced a variety of TechCasts (www.newark.com/techcast), online seminars that act as short training modules that introduce parts and technology to engineers. "TechCast makes design information about our supplier products available to our engineers 24/7," says Jeff Hamilton (**photo**), director of marketing for design services at Newark. "Designers are embracing the Web."

Newark in February introduced 110 TechCasts and has since added to its list at a rate of about 20 seminars per month. Although the content of the TechCasts comes from suppliers, Newark produces them internally to ensure that the modules serve the purpose of education, not marketing. "They offer system-level-design insight. They're not a vehicle for new-product advertisements," Hamilton says. The seminars average just 10 to 20 minutes each. This format is attractive to suppliers, which realize that their customers need quick access to technical information, not long seminars.

In addition to its own Avnet OnDemand (www.avnetondemand.com) online-educational portal, Avnet Inc (www.avnet.com) offers a range of in-person training workshops that teach new technology. The distributor offers SpeedWay workshops that include full-day training and On-Ramp seminars that usually range from one to two hours each. Avnet offers many of these workshops at customers' facilities. "We have SpeedWay seminars with full-day sessions, and our customers walk out with hardware that's already validated," says Rafael Cruz, vice president and director of design services at Avnet. "Customers can bring a design problem and get a hands-on deliverable."

—by Rob Spiegel

OUTLOOK

PC-TV-TUNER MARKET FACES STATIC

In-Stat (www.instat.com) expects unit shipments for PC-TV tuners this year to decline by nearly 11% from 2008's level due to shrinking demand and the worldwide economic recession. The research company reports that the market also faces fundamental challenges, including slow consumer demand, increased competition from online TV and other programming sources, and lower prices due to a shift from hybrid-analog/digital tuners to digital-only tuners.

"Opportunities for growth will be for hybrid-analog/digital-tuner manufacturers to increase share by lowering prices or for new entrants to leapfrog the analog and hybrid segments by aggressively targeting the emerging digital-only segments, albeit with lower margins," says Gerry Kaufhold, an In-Stat analyst. "Overall, selling PC-TV tuners is going to be a tougher business."

In-Stat notes that Microsoft's Windows 7 and the new version of Media Center will include better connectivity for PC-TV tuners, which could encourage sales. The company expects moderate unit growth to resume next year, thanks to digital-only-tuner shipments, but says that worldwide PC-TV-tuner revenue likely peaked in value at about $1.4 billion during 2008.**–SD**

GREEN UPDATE

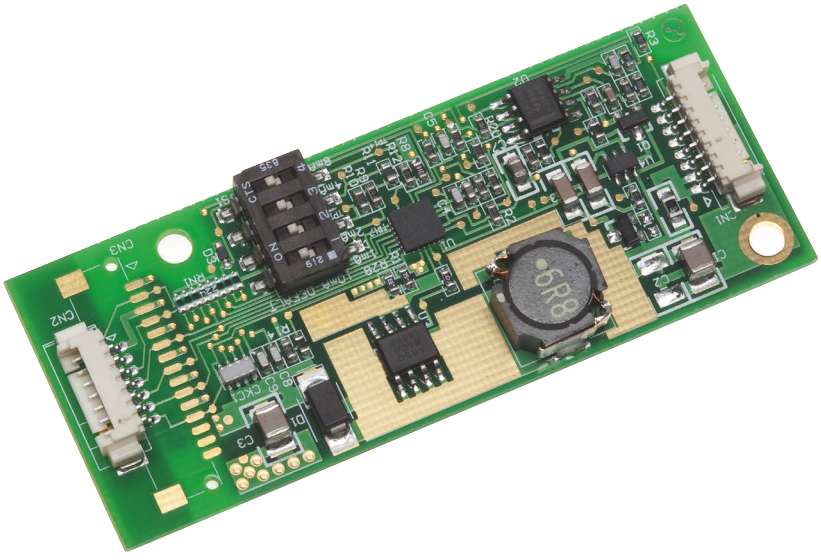
ENERGY STAR 5.0 IS IN EFFECT

The EPA's (Environmental Protection Agency, www.epa.gov) Energy Star 5.0 Specification for Computers went into effect on July 1, 2009. The specification applies to desktop, notebook, and thin-client systems. The EPA finalized the specification, which went through the EPA's standard comment period, on Nov 14, 2008. Comments from stakeholders encouraged including in the specification clarification of a full network connectivity definition, a sliding scale for graphics capability in desktops to provide for discrete GPUs (graphics-processing units) and associated capability, and guidance on wireless-radio and hard-drive-power-management status during idle testing.

The EPA reports that development of the specification's game-console requirements will continue through the year. With the effective date for consoles scheduled for July 1, 2010, the EPA also aims to engage game publishers when finalizing requirements for the specification to ensure that games do not hinder console-power management. The process to qualify computers will be generally consistent with what was in place for Version 4.0 of the specification, with a requirement for an active manufacturer partnership and the collection of data through the EPA's OPS (online-product-submittal) tool at www.energystar.gov/ops.**–SD**

productroundup

OPTOELECTRONICS/DISPLAYS



Driving systems targets midsized LED-backlit panels

Based on the vendor's LX1996 LED driver, the LXMG1960-28 backlight-driving integrated plug-and-play system suits midsized LED-backlit panels. Aiming at LCD televisions, notebook computers, automotive, and other display platforms and applications, the module consists of a boost converter and six programmable precision current sinks. The system drives as many as six strings of LEDs with string-to-string current matching of 1% for panel-brightness uniformity. A dedicated input pin works with an external thermistor, providing output-current foldback to protect the LEDs in overtemperature scenarios. Additional features include a 4.75 to 28V input voltage and support for dc-voltage, PWM-signal, and potentiometer-dimming methods, along with a combination of analog and digital dimming, providing a 1000-to-1 dimming ratio. Available in an ROHS-compliant package, the LXMG1960-28 costs $10 to $15.

Microsemi Corp, www.microsemi.com

Logic-gate optocouplers suit aerospace and military applications

The ACPL-570xL/573xL/177xL series of hermetically sealed, high-gain optocouplers includes single-, dual-, and quad-channel devices. The 3.3V logic-gate devices enable operation over a −55 to +125°C temperature range, meeting aerospace, industrial, and military applications. The optocouplers allow designers to use low-power components, suiting microprocessor-system interfaces, process-control I/O isolation, voltage-level shifting, and logic-ground isolation. The devices reduce or eliminate the need for extra interface components or voltage converters. Each channel contains a GaAsP LED and an integrated high-gain photon detector. A high-gain output stage features an open-collector output, enabling lower saturation voltage and higher signal speed than do typical photo-Darlington optocouplers. The supply voltage for the optocouplers suits operation as low as 3V with no adverse effects on parametric performance. Devices in the series cost $43 (1000) each.

Avago Technologies, www.avagotech.com

Constant-current controller suits use with triac phase-control wall dimmers

The LM3445 constant-current controller uses a forward- or reverse-phase-controller triac to enable offline, uniform, flicker-free dimming of high-brightness LEDs. The device has a 100-to-1 range of dimming capability and maintains a 1A constant current to LEDs. The driver interfaces with resistive loads, such as incandescent or halogen light bulbs. An LED bulb does not appear as a resistive load to the wall dimmer, so dimming an LED bulb using a typical triac dimmer yields suboptimal performance. The LM3445 translates the triac-chopped waveform to a dim signal and decodes the signal for a full range of uniform, flicker-free dimming, preventing 120-Hz flicker and the limited dimming range of many other LED drivers. The LM3445 constant-current controller costs $1.75 (1000).

National Semiconductor, www.national.com

LED-backlighting strips illuminate small and mid-sized displays

The OPA775 and the OPA776 LED-backlighting-strip series feature white LEDs and suit illumination of small and midsized displays requiring lighting intensity and reliability. Operating at 12V, the OPA775 includes a strip of 7.5-in. FR-4 board with three LEDs with one to 30 strips connected per bus. The strips feature Zierick 1286T connectors, allowing the "Jacob's ladder" construction and enabling

30 strips to draw a total of 3.75A current. The OPA776 backlighting strips meet the OPA775 performance at 24V operation. An OPA776 comprises two 7.5-in. FR-4 board strips with three LEDs per strip and a jumper-wire connection. The strips come in sets of 60 and draw a total current of 3.75A. The OPA775 and the OPA776 have a 50-lumen-per-strip luminous flux, with a 125-mA drive current to each LED. The vendor crimps the bus wires during manufacturing and spaces the LED strips at 6-in. intervals. Prices for the OPA775 backlighting-ladder-strip series range from $5.58 to $5.70 (1000); prices for the OPA776 series range from $10.85 to $11.18 (1000).

Optek Technology, www.optekinc.com

COMPUTERS AND PERIPHERALS

Graphics accelerator has 320 unified stream-processing units

Based on a new-generation GPU with 320 unified stream-processing units, the ATI FireProT V7750 graphics accelerator provides 1 Gbyte of frame-buffer memory and a 30-bit display pipeline. Features include multiple DisplayPort outputs and a Dual-Link-enabled DVI output, enabling a multimonitor desktop that is more than 5000 pixels wide in a single-slot form factor. The ATI FireProT V7750 graphics accelerator costs $899.

Advanced Micro Devices, www.amd.com

XMP DDR3 laptop memory runs at 1066 MHz and CL5

Targeting notebook PCs using Intel's Cantiga mobile chip set, the XMP HyperX DDR3 SO-DIMMs come preprogrammed with JEDEC and XMP profiles. The Intel-certified modules run at 1066 MHz and CL5 (column-address-strobe latency of five). The 4-Gbyte, 1066-MHz, low-latency kit of two XMP HyperX DDR3 SO-DIMMs costs $212.

Kingston Technology, www.kingston.com

Hard drive uses 500-Gbyte-platter technology

Using 500-Gbyte-platter technology, the Caviar Green 2-Tbyte hard drive features a 32-Mbyte cache and a 100-Gbps/in.^{2} area1 density. The drive suits use in USB, FireWire, and eSATA hard drives and desktop-RAID environments and costs $299.

Western Digital, www.wdc.com

EDN ADVERTISER INDEX

EDN provides this index as an additional service. The publisher assumes no liability for errors or omissions.

BY DAVID WILLIAMS • WHIRLPOOL

A breath of fresh air

DANIEL VASCONCELLOS

It was a quiet day when my manager came to me with an urgent request. Our most recent quality numbers showed a significant regression, causing the failure rates of our control boards to more than triple in three months! As this fact became better known, the number of fingers pointing at the engineers to fix this issue increased exponentially. Management assigned a team of engineers to look for anything that could have changed. Did we make any component or process changes? Was the regression within normal statistical variation? Was there a change in the reporting structures? The answer to all these questions was no.

With nothing to show for our first investigation, we ordered many "failed" controls from the service department. While waiting for controls from the service department to analyze, we called customers and service technicians to get more info on why they were replacing these controls. Many customers would say only that the control boards failed intermittently, would not respond to key presses, or would randomly just stop. Service techs were not much help, either, often preferring a "swaptronics" approach to troubleshooting, rather than detailed root-cause analysis.

Finally, the first 10 boards arrived, and, as engineers, we eagerly attempted to uncover the issue, fix it, and put this whole thing behind us. Strangely, all 10 boards worked as we expected with no issues. The same scenario occurred with the next 10, the 10 after that, and so on until we had analyzed more than 50 boards and still had no idea what was causing the problem.

With the work becoming more and more hopeless, a batch of controls came in for review. I went about analyzing the boards, and the first few checked out fine. Then, I finally got one board that actually was malfunctioning.

I isolated the issue to a tactile switch that was not working as expected. Upon further inspection, I noticed some contamination on a hidden shelf between the opposite-polarity leads of the switch. Examination of another failing board confirmed the presence of this foreign material, which looked like flux contamination. The mixture of this contamination with the metals, voltage bias, and local humidity in that area had caused electrochemical migration, creating dendrites of the local metals. These dendrites, in turn, had slowly shorted out the switch. When I brought another engineer into the lab, though, all the failing boards were functioning perfectly fine.

After some good-natured ribbing from the other engineer, I again looked into the boards. A board had started to fail again. Taking another board and breathing across a suspicious switch caused it to also start failing. The film of condensed water molecules from my breath, in conjunction with the lower resistive path that the dendrites had caused, made the overall resistive path small enough to affect the circuit's performance. Those previous controls tested OK because they had dried out before I tested them.

It turns out that, about the time of the regression, the company had contracted with a new supplier for the switch, but no one ever notified the engineers of the change. The new part was more susceptible to contamination due to spacing and construction, which caused the increased field failures.

Despite the good-natured ridicule I'd received for the "breath test," it nonetheless was an effective way to run a quick environmental-condensation test, stressing controls and finding issues. EDN

David Williams is a senior engineer at Whirlpool (St Joseph, MI).

www.edn.com/tales

FREE WEBCAST

SIGNAL INTEGRITY DESIGN

USING FAST CHANNEL SIMULATION AND EYE DIAGRAM STATISTICS

>>> *THIS WEBCAST WILL DEMONSTRATE THE "WHAT IF" DESIGN SPACE EXPLORATION WORKFLOW THAT OUR NEW MILLION-BIT-PER-MINUTE CHANNEL SIMULATOR AND EYE DIAGRAM TOOL ENABLES.*

DATE: July 29, 2009 **TIME:** 11AM PT / 2PM ET

PRESENTER: Sanjeev Gupta

Signal Integrity Applications Expert, *EEsof EDA Division, Agilent Technologies.*

Improvements to traditional SPICE-type simulation have increased signal integrity channel simulation speeds to thousands of bits per minute. An overnight run can create a million-bit eye diagram and the associated metrics and statistical figures of merit. But signal integrity engineers need to repeat this determination for thousand of points in the design space in order to select the optimum combination of, for example, pre-emphasis, channel characteristics, and equalizer. Therefore, optimization using eye diagram goals requires a channel simulation technique that is orders of magnitude faster than even the fastest SPICE.

REGISTER TODAY

TMWorld.com/Webcasts

Sponsored by:

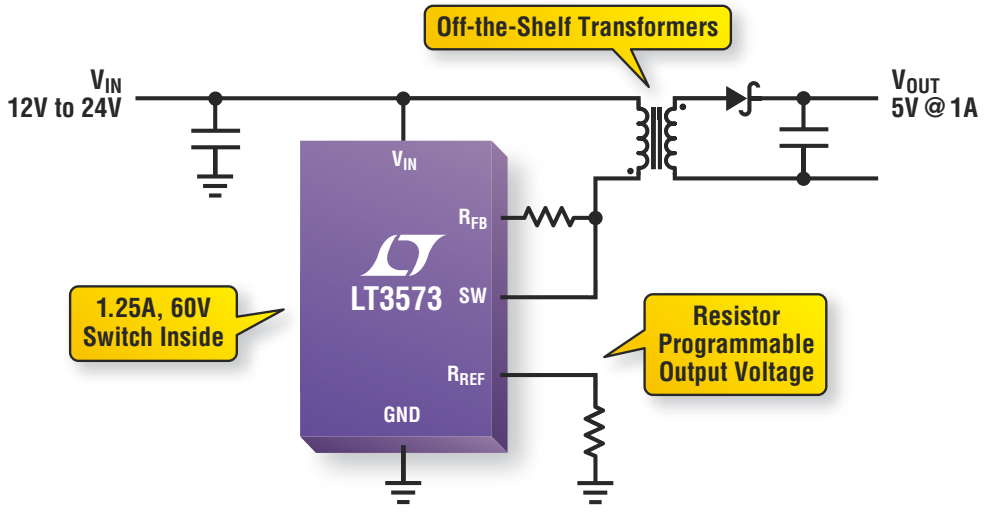
Agilent Technologies

Produced by:

Test & Measurement World

EDN

Isolated Flyback–No Opto



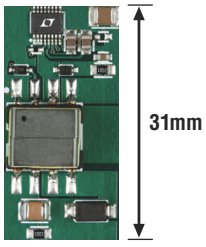
Off-the-Shelf Transformers and Low Parts Count

The LT®3573 is an easy-to-use monolithic flyback converter that greatly simplifies isolated DC/DC converter design. It has an input voltage range of 3V to 40V and can deliver up to 7W of output power. Off-the-shelf transformers can readily be used and its boundary mode operation simplifies the design and improves regulation. A growing number of new applications demand isolation to ensure ground separation from a noisy bus voltage for noise-sensitive applications including GPS systems, hybrid electric vehicles, displays, programmable logic controllers and medical systems.

Features

- 3V to 40V Input Voltage
- No Optocoupler Required
- No 3rd Transformer Winding Required
- ±3% Load Regulation
- Low Parts Count
- Internal 1.25A/60V Switch

LT3573 Demo Circuit (Actual Size)



Info & Free Samples

www.linear.com/3573

1-800-4-LINEAR

Free Automotive Electronics Solutions Brochure

www.linear.com/autosolutions

LINEAR TECHNOLOGY